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NBSIR 79-1756

Measurement Techniques for High Power Semiconductor Materials and Devices: Annual Report, October 1, 1977 to September 30, 1978

F. F. Oettinger, Editor

Electron Devices Division
Center for Electronics and Electrical Engineering
National Engineering Laboratory
National Bureau of Standards
Washington, DC 20234

Issued June 1979

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Center for Electronics and Electrical Engineering
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PREFACE

This work was conducted as a part of the Semiconductor Technology Program of the National Bureau of Standards (NBS). This program serves to focus NBS research to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in measurement technology for use in specifying materials and devices in national and international commerce and for use by industry in controlling device fabrication processes. This research leads to carefully evaluated and well-documented test procedures and associated technology. Special emphasis is placed on the dissemination of the results of the research to the electronics community. Application of these results by industry will contribute to higher yields, lower cost, and higher reliability of semiconductor devices. Improved measurement technology also leads to greater economy in government procurement by providing a common basis for the purchase specifications of government agencies and, in addition, provides a basis for controlled improvements in fabrication processes and in essential device characteristics.

The segment of the Semiconductor Technology Program described in this annual report is supported by the Division of Electric Energy Systems of the Department of Energy (DOE) under DOE Task Order A021-EES, Amendment No. 2. Previous work reported under this DOE Task was on a calendar year basis. Beginning with this Annual Report, reporting will be on a fiscal year basis; thus there is a three-month overlap between the last annual report and this one. The contract is monitored by Dr. Russell Eaton of DOE. The NBS point of contact for information on the various task elements of this project is F. F. Oettinger of the Electron Devices Division at the National Bureau of Standards. The work reported herein also drew upon the results of studies carried out under other parts of the Semiconductor Technology Program which were funded by the Defense Advanced Research Projects Agency under Order No. 2397, Program Code 7D10, and by the NBS.

Disclaimer

Certain commercial equipment, instruments, or materials are identified in this report in order to specify adequately the experimental procedure. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material or equipment identified is necessarily the best available for the purpose.

Measurement Techniques for High Power Semiconductor Materials and Devices

ANNUAL REPORT
October 1, 1977 to September 30, 1978

F. F. Oettinger, Editor

EXECUTIVE SUMMARY

This annual report describes results of NBS research directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from the rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for materials for thyristors and rectifier diodes. Application of this measurement technology will, for example, enable industry to make devices with higher individual power-handling capabilities, thus permitting very large reductions in the cost of power-handling equipment and fostering the development of direct current (dc) transmission lines to reduce energy waste and required rights-of-way.

The major tasks under this project are (1) to evaluate the use of thermally stimulated current and capacitance measurements and other deep level measurement techniques as a means for characterizing lifetime-controlling or leakage source defects in power grade silicon material and devices and (2) to develop procedures to enable spreading resistance measurements of thyristor starting material and layer profiles to be made on a reliable basis.

Deep Level Measurements — The presence of deep level impurities in semiconductor power devices is a consequence of their unintentional introduction during the wafer fabrication procedure or their intentional introduction in order to adjust the switching properties of the device. In either case, the dominant effect of the deep level is to modify the minority carrier lifetime. Measurement techniques to detect, characterize, and identify such deep levels are required in order to monitor the presence of unintentional contamination or to characterize fully and understand the behavior of intentional ones. The use of such techniques for process diagnostics would enhance the manufacturer's ability to control the quality (yield, reliability, and cost) of his product.

The effective utilization of these measurement methods to the design and fabrication of power devices has several prerequisites: 1) the ability to fabricate test structures on starting and in-process material for the purpose of deep level studies, 2) the establishment of well-characterized measurement procedures and methods for analyzing data, and 3) establishment of the relationship between the presence of deep levels and electrical device parameters. Research efforts during this contract period were aimed at satisfying these requirements.

Development of procedures for the fabrication of test structures on diffused thyristor wafers was completed. The basic process consists of mesa formation by plasma etching, passivation with a deposited silicon dioxide, and contact metallization. These fabrication procedures utilize no steps requiring temperatures higher than 400°C. A new test pattern (NBS-20) was designed to implement these fabrication procedures, and resulting devices were evaluated.

Deep level measurement procedures established during the previous contract period were implemented and demonstrated during this contract period. The two levels of sulfur in silicon were used as the measurement vehicle and were characterized in detail using the developed procedures. The critical dependence of these measurements on thermometry has been established, and an improved technique to decrease temperature uncertainties was implemented. Use of the procedures for deep level measurements and the improved precision in temperature measurement enabled the detection of an isotope shift in the midgap energy level of sulfur.

By utilizing the previously developed variable-temperature wafer probing apparatus, a variety of device parameters were measured as a function of wafer position. Wafer maps of reverse leakage current, forward voltage drop, diode reverse recovery lifetime, open circuit voltage decay lifetime, and defect density were made; direct correlations were observed.

Spreading Resistance Measurements — Knowledge of the resistivity (dopant) variations which exist in a semiconductor structure is of primary importance for use in design and modeling of the structure and for quality control during its fabrication. Most such resistivity variations are intentional resulting from device fabrication procedures such as thermal diffusion or ion implantation. Some, however, are unwanted and are due to loss of process control or to microsegregation effects during crystal growth, as, for example, in the n-base region of a thyristor fabricated in float-zoned silicon.

The spreading resistance technique, although destructive in that contact damage is incurred, is presently the primary method for measuring resistivity variations in silicon material and devices. This technique, which has been in use for a number of years in the semiconductor industry, is based on the constriction resistance of pressure contacts between small metal probes and the semiconductor bulk material or multilayered device structure of interest. The technique gains its widespread usefulness from a unique combination of performance characteristics: lateral spatial resolution of about 5 μm, effective depth resolution of about 20 nm, and a dynamic resistivity response of 8 or 9 orders of magnitude for both n- and p-type silicon. The spreading resistance technique has undergone steady improvement in precision and accuracy. However, it has had noticeable shortcomings, including some that are virtually unique to measurements on thyristors and related high-power control devices. Those shortcomings which related to control of the (111) n-type silicon specimen surface to obtain acceptable measurement precision and to calibration of the measurement for p-type dopants commonly used in thyristor fabrication were successfully addressed during the contract period.

The repeatability of spreading resistance measurements on high resistivity n-type silicon has been observed to be unsatisfactory in many laboratories. The effect of this on power device fabrication is twofold: 1) loss of reliability of measurements of starting crystal uniformity and 2) uncertainty whether apparent shifts in n-base resistivity, sometimes observed after device fabrication, are real or simply measurement artifacts. The cause of the unsatisfactory measurement was believed to be improper preparation of the silicon specimen surface which resulted in loss of control of the metal probe-semiconductor contact properties.

Several methods for preparing the silicon specimen surface were investigated for bulk silicon specimens in the resistivity range from 30 to 400 Ω·cm. Polishing with either 0.5- or 3-μm particle size diamond suspended in a nonaqueous fluid was found to be clearly superior to traditional chem-mechanical polishing methods with silica in basic aqueous solution. The superiority obtained by diamond polishing is evidenced by greatly improved reproducibility of average spreading resistance values following specimen repolishing, by less point-to-point measurement scatter on any one specimen surface and by reduced sensitivity of measurements to specimen treatment subsequent to polishing. Of the two polycrystalline diamond polishes tested for top surface polishing, the one with the smaller diamond particle size (0.5 μm) was adopted as the preferred method of specimen preparation. This choice was based

primarily on a higher quality specimen surface (lighter scratch damage) obtained with the 0.5-μm diamond.

The use of diamond was also applied to bevel-sectioning of thyristor devices for depth profiling. However, the beveling process must be done against a harder surface than is used for top surface polishing in order to maintain flatness of beveled surface and sharpness of beveled surface interface. It was found necessary when using such a hard work surface to use a still smaller size diamond, 0.1 μm, for beveling to maintain measurement quality. Measurements on diamond-beveled devices retain high repeatability for the n-base layer and give good agreement with silica-beveled and baked thyristor sections for the cathode emitter and p-base layers.

Tests were made of the equivalence of spreading resistance response on bulk specimens of silicon variously doped with boron, aluminum, or gallium at levels typical of those used in thyristor diffusions. Spreading resistance data acquired during these tests clearly show that boron-doped silicon specimens, which are readily available, can be reliably used to calibrate spreading resistance measurements on silicon doped with gallium or aluminum. It has been customary to assume this equivalence, but it had not been demonstrated previously.

1. INTRODUCTION

This project is directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high-power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for materials for thyristors and rectifier diodes.

The project is designed to provide, disseminate, and foster the standardization of improved measurement methods required in high-power semiconductor technology, for use in specifying materials and devices in commerce, and by industry in controlling device manufacturing processes, and in designing systems. Application of this measurement technology will, for example, enable industry to: (1) make power semiconductor devices with greater uniformity of characteristics, thus permitting improvements in parallel and series connections of devices for applications from fusion generation to ac/dc conversion, (2) make devices with higher individual power handling capabilities, thus permitting large reductions in the cost of power handling equipment and fostering the development of dc transmission lines to reduce both energy waste and the extent of required rights-of-way, and (3) provide devices, and the systems utilizing them, with the reliability and performance required in energy generation, utilization, and conservation.

The major tasks under this project are (1) to evaluate the use of thermally stimulated current and capacitance measurements and other deep level measurement techniques as a means for characterizing lifetime-controlling or leakage source defects in power grade silicon material and devices and (2) to develop procedures to enable spreading resistance measurements of thyristor starting material and layer profiles to be made on a reliable basis.

2. DEEP LEVEL MEASUREMENTS

by

R. Y. Koyama J. Krawczyk
W. E. Phillips Y. M. Liu
D. R. Myers*

2.1 Objectives

The overall objective of this task is to evaluate the use of thermally stimulated current and capacitance measurements (TSM) and other deep level measurement techniques for characterizing defects which control leakage current and lifetime in power grade silicon materials and devices. Phases 1 and 2 of this continuing task were completed in September 1976 and September 1977, respectively. Phase 3 of the task, October 1977 through September 1978, had the following objectives:

2.1 Complete the development of the fabrication procedures used to produce mesa diodes. These procedures are to be compatible with thyristor manufacturing procedures so that they can be used routinely to analyze and control manufacturing processes using deep level measurement (DLM) techniques.

2.2 Establish routine procedures for utilizing TSM (dynathermal and isothermal) and analyzing TSM data with emphasis on investigation of the metrological aspects of the measurement method associated with midgap defect centers which control the carrier lifetime. Defects such as gold or platinum (common lifetime killers) or other purposely introduced defects will be used as study vehicles in establishing these procedures.

2.3 Develop capabilities to measure electrical parameters of devices (fabricated test structures such as p-n junctions and MOS capacitors, and commercial devices such as rectifiers and thyristors) so that the parameters can be related to the presence of defects.

This report discusses the progress that has been made in each of these objective areas during the period October 1977 through September 1978.

2.2 Background

Deep level defect measurements such as TSM [2-1] and deep level transient spectroscopy (DLTS) [2-2] utilize the ability of active defects in depletion regions to trap carriers and to emit them after receiving

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*NBS-NRC Postdoctoral Research Associate.

sufficient thermal energy. Suitable analysis of the measured data allows determination of the density, energy level, and emission rate of the defect. The interest in measurement of deep levels in semiconductors, particularly in application to power devices, stems from two related aspects: 1) detection, identification, and control of unwanted intrinsic or process-induced impurities or defects; and 2) characterization and control of defects specifically introduced for lifetime control. These techniques, which have generally been confined to laboratory studies of packaged devices, have now been extended to measurements on devices in wafer form [2-3], and routine procedures for measurement and analysis of data have been established so that these techniques can be utilized as diagnostic tools in the fabrication area as well as in the research laboratory.

The approach in this program has been twofold. Apparatus has been developed to permit deep level measurements on both packaged devices (TO-5) and full-sized wafers. Although the developed measurement techniques are fully applicable to either device format, each offers distinctive advantages. The packaged device format permits much higher precision in thermometry; this in turn allows more precision in the measurement of emission parameters and energy levels. Although such measurements can also be done on the full-wafer apparatus, this equipment is more suited for mapping of such parameters as deep level defect density and a variety of electrical device parameters. In addition, where it is used as a diagnostic tool in the manufacturing of power devices, the wafer probing apparatus offers the advantage of allowing deep level measurements to be made on processed wafers without waiting for the time-consuming packaging step.

2.3 Accomplishments This Year

2.3.1 Test Structure Development (Objective 2.1)

The objective of these studies is to develop a procedure which can be used to fabricate diode test structures on diffused power device wafers for the purpose of diagnostic measurements by deep level detection techniques. Preliminary investigations which established the general procedures and outlined a variety of techniques were reported previously [2-4, pp. 31-38]. A primary consideration in the development of these procedures is to minimize or eliminate the use of high temperature treatments on the test wafer in order to avoid alteration of the wafer characteristics. In order to compare and evaluate various process procedures, mask set NBS-13 was designed and implemented.

The basic test structure to be fabricated is a mesa diode utilizing one of the two p^+n junctions of a basic thyristor wafer which has undergone the first diffusion step (see fig. 2-1). Due to the deep diffusions of typical high power thyristor structures, the mesa diode test structures may require removal of as much as 80 to 100 μm of material in order to isolate the junction. Junction isolation is followed by the application of a junction passivation and protection layer; metal contacts are then applied to complete the procedure.

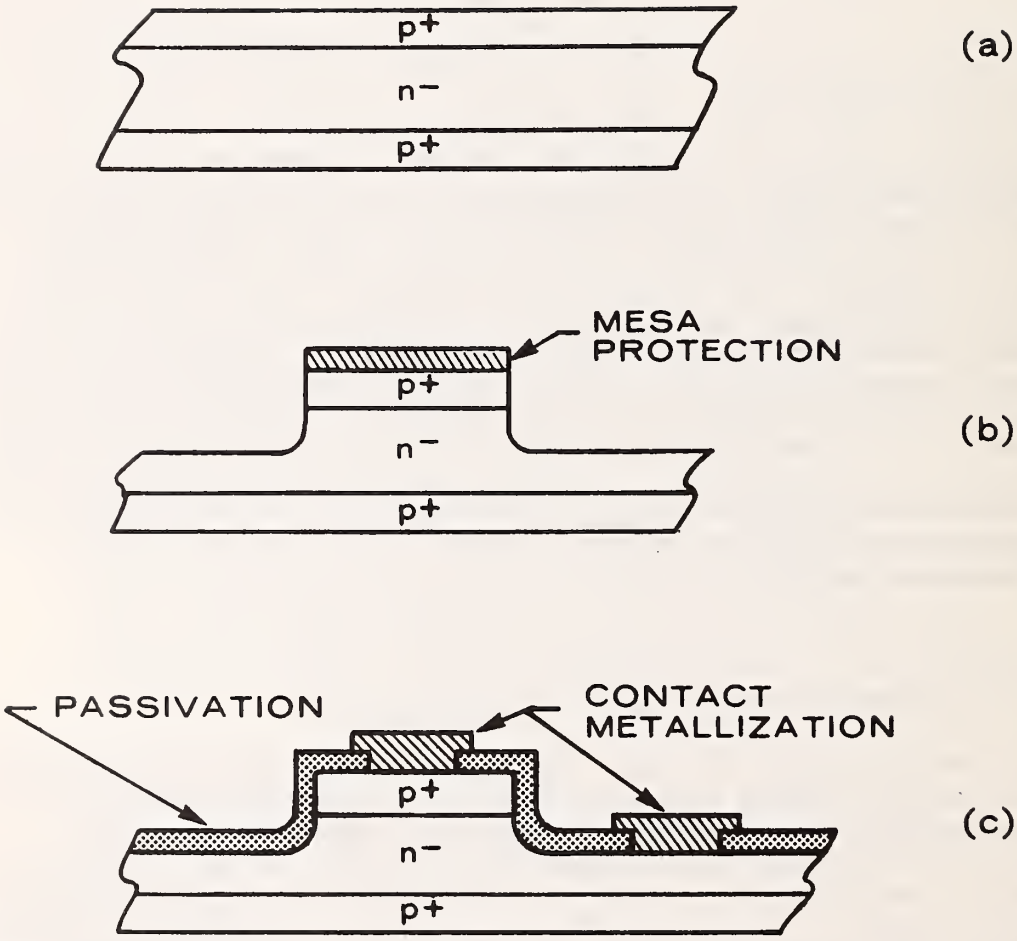


Figure 2-1. The basic mesa diode processing steps: a) starting wafer; b) mesa protection, junction isolation; c) passivation, contact cut, and metallization.

During this contract period, most of the effort on this task was devoted to evaluating mesa etching procedures and junction passivation techniques. In terms of routine fabrication and repeatability, these two steps are considered the most important. The mesa etching procedure must be controllable in order to assure proper etching depths for the diode structures. Mesa etching techniques which were evaluated included ultrasonic machining, chemical etching, and plasma etching. The plasma etching technique was found to be the most reproducible procedure and provided mesas of high quality. The passivation of the junction following the mesa etch is an important step to assure devices of low leakage characteristics which are required for the deep level measurements. This was successfully accomplished with the use of chemical-vapor-deposited silicon dioxide.

The following two sections give, respectively, the detailed procedure for fabricating mesa diodes on diffused thyristor wafers and the results of an evaluation measurement mode on a mesa diode using the developed procedures. Some additional details describing the mesa etching procedure (ultrasonic and plasma methods), the mesa passivation procedure, and contact metallization are given in Appendix A.

The use of test pattern NBS-13 [2-4, pp. 34-36] was extremely successful in providing information to allow judicious choices among the alternative processing techniques that were available. In addition, it revealed the advantages and limitations of both the processes and the test structures that were used in the fabrication procedures. One of the major limitations of the plasma etching procedure revealed by processing with test pattern NBS-13 was the high rate of lateral etch (undercutting). For the small structures on test pattern NBS-13, this resulted in poorly defined mesa areas. In order to compensate for this lateral etching, a different test pattern, designated NBS-20, was designed. Test pattern NBS-20 consists of square mesa diodes of dimensions 2.54 by 2.54 mm, spaced in a square array at 5.08-mm intervals. The contact and metallization masks are designed with wide tolerances to allow for lateral etching and ease of mask alignment. Figure 2-2 shows photographs of the eight levels of a single diode in test pattern NBS-20. As in the case of test pattern NBS-13, additional mask levels were included in this set to allow for process variations or alternative contact schemes. Each level is identified in the figure.

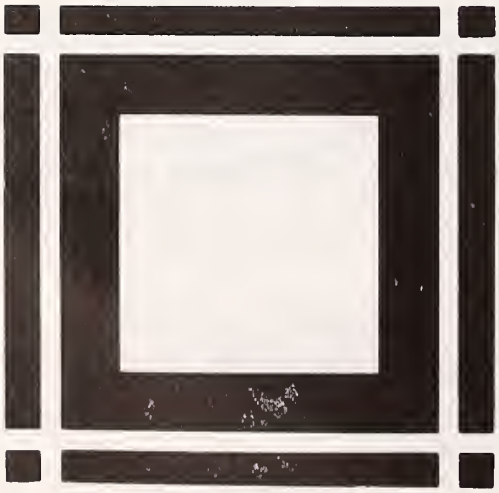
A Mesa Diode Fabrication Procedure - This section details a procedure which has been used to fabricate mesa diodes with electrical and physical properties which are suitable for deep level measurements. The starting wafer is assumed to have undergone the first high temperature diffusion step to yield a $p^+n^-p^+$ wafer structure.

1. Wafer Preparation

   The diffused wafers are first chem-mechanically polished on one side. The amount of material to be removed depends on the depth of the p^+-diffusion. It is necessary that the diffused material not be removed completely; generally only enough mate-

1. MESA

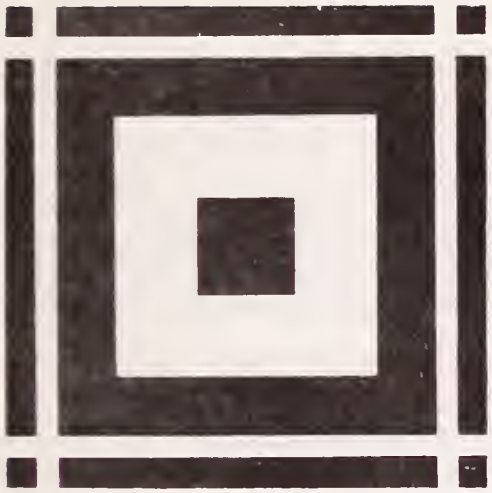
2. n-CONTACT/DIFFUSION



3. n-METAL

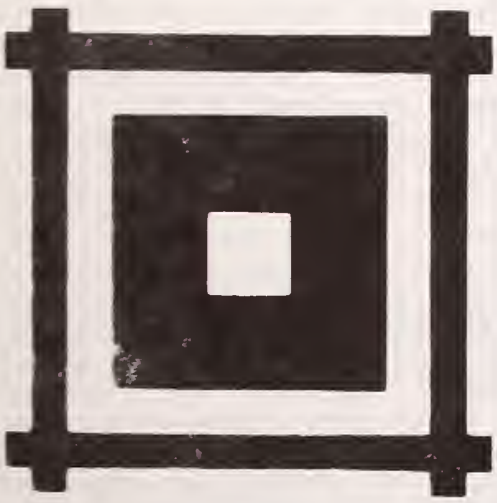
4. p-CONTACT

Figure 2-2. Photomicrographs of the eight mask levels of a single diode on size is 5.08 by 5.08 mm.

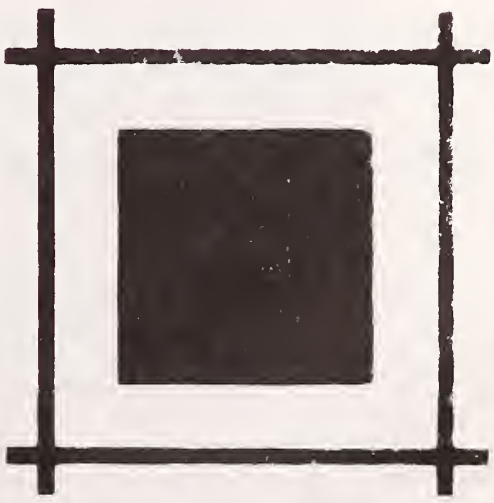


5. np-METAL

6. np-METAL WITH GATE



7 np-CONTACT



8 n METAL

test pattern NBS-20. The mesa (level 1) is 2.54 by 2.54 mm and the overall die

rial to achieve a reasonable polish is removed. The principle reason for this operation is to avoid liftoff of the aluminum masking material during plasma etching. The polished surface also aids in the alignment procedures during masking operations.

2. Wafer Cleanup

The wafers are first etched in a 1:1:2 solution of ammonium hydroxide, hydrogen peroxide, and water ($NH_4OH:H_2O_2:H_2O$) for 20 min at 50°C; then they are rinsed in deionized water for 10 min at 23°C (hereafter called "rinsed"). Next, they are etched in a 1:1:2 solution of hydrochloric acid, hydrogen peroxide, and water ($HCl:H_2O_2:H_2O$) for 20 min at 50°C, then rinsed. Finally, they are etched in a 1-percent hydrofluoric acid (HF) solution for 30 s at 23°C, rinsed, and blown dry with nitrogen.

3. Plasma Etching Procedure

Aluminum is evaporated onto the polished surface of the wafers to a thickness of 1000 nm by an electron-gun evaporator. The mesa areas are then defined on the aluminum layer by photolithography (level 1, NBS-20). Following the spin-on application of 1.5 to 1.0 μm of positive photoresist (KTI-II* with a viscosity of 25 centistokes is found to be satisfactory), the wafers are baked for 20 min at 75°C. The resist is then typically exposed for 20 s and developed for 30 s, and then rinsed. This is followed by a 20-min bake at 120°C. The aluminum metal is then etched in a 20:5:1 solution of phosphoric acid, water, and nitric acid ($H_3PO_4:H_2O:HNO_3$) (hereafter called "aluminum etch") for about 8 min at 23°C and then rinsed. Finally, the resist is stripped with acetone, and then the wafers are rinsed. The wafers are placed in the plasma etching system and processed for the time required to obtain the desired etch depth; this time is chosen from a previously established calibration of etch depth *vs.* time. Following plasma etching, the aluminum "caps" protecting the mesa regions are removed in warm (35 to 40°C) aluminum etch and the cleanup procedure given in step 2 above is repeated.

4. Passivation-Protection Layer

The wafers are etched for 30 s in an ice-bath cooled solution of CP-6 (nitric acid, hydrofluoric acid, and acetic acid, $HNO_3:HF:CH_3COOH$, 5:3:4) and then rinsed and blown dry with nitrogen. The wafers are then placed in a chemical vapor deposition reaction system. The chemical-vapor-deposited silicon dioxide (CVD-SiO_2) is formed by the pyrolytic decomposition

*KTI Chemicals, Inc., Sunnyvale, CA 94086.

of 4-percent silane (SiH_4) in nitrogen (N_2) flowing at 0.28 standard liters per minute (sLpm), oxygen (O_2) flowing at 0.025 sLpm, and nitrogen (N_2) flowing at 20 sLpm. The wafers are preheated and held at 400°C during deposition. The deposition rate is approximately 40 nm/min; final thicknesses in the range from 600 to 800 nm were used.

5. n^--Contact Metallization

Using photolithographic techniques, the CVD-SiO_2 is etched to expose the appropriate n^--regions of the wafer (level 2, NBS-20). Buffered-HF at room temperature is the etchant, and typical thicknesses of CVD-SiO_2 require 20 to 25 min of etching time to reach the silicon. The wafers are then rinsed, dried, and immediately placed in the evaporator bell jar. About 200 nm of gold (doped with 0.6% Sb) is filament-evaporated onto the front surface. The gold layer is then microalloyed at 400°C for 20 min in nitrogen to form the contact. Following this, the gold layer is photolithographically defined (level 3, NBS-20) for the n^--contacts.

6. p^+-Contact Metallization

Contact cuts through the CVD-SiO_2 layer on top of the mesas are photolithographically defined with level 4 of NBS-20. Aluminum metal is e-gun evaporated over the front surface and then photolithographically defined with level 5 of NBS-20.

Figure 2-3 shows a photomicrograph of a mesa diode fabricated with levels 1, 2, 3, 4, and 5 of test pattern NBS-20. The following areas are identified: 1) aluminum on p^+-silicon; 2) CVD oxide on p^+-silicon; 3) CVD oxide on n^--silicon; 4) aluminum on gold (0.6% Sb) on n^--silicon (see discussion in Appendix A-3 regarding the possible formation of gold-aluminum intermetallic compounds); and 5) cell boundaries, CVD oxide on n^--silicon.

The procedure detailed above has been successfully used to fabricate mesa diode structures with reverse leakage significantly less than 1 μA with applied bias exceeding 30 V. These would be suitable for deep level measurements. As an example, figure 2-4 displays thermally stimulated capacitance and current curves for a mesa diode fabricated on a thyristor wafer whose p^+-diffusions were 90 μm deep from each surface. The measurements were made on the wafer probing apparatus with a heating rate of about 5 K/s. There are two distinctly resolved emissions near 115 and 135 K; the low temperature tail on both curves implies the existence of at least a third level. These levels are all electron emitters in the upper half of the silicon band gap in the lightly doped n^--region of the $p^+n^-p^+$ wafer. Although detailed measurements to determine the energy, origin, and identity of these levels have not been made, these results demonstrate the validity of the procedures used to fabricate the mesa diodes.

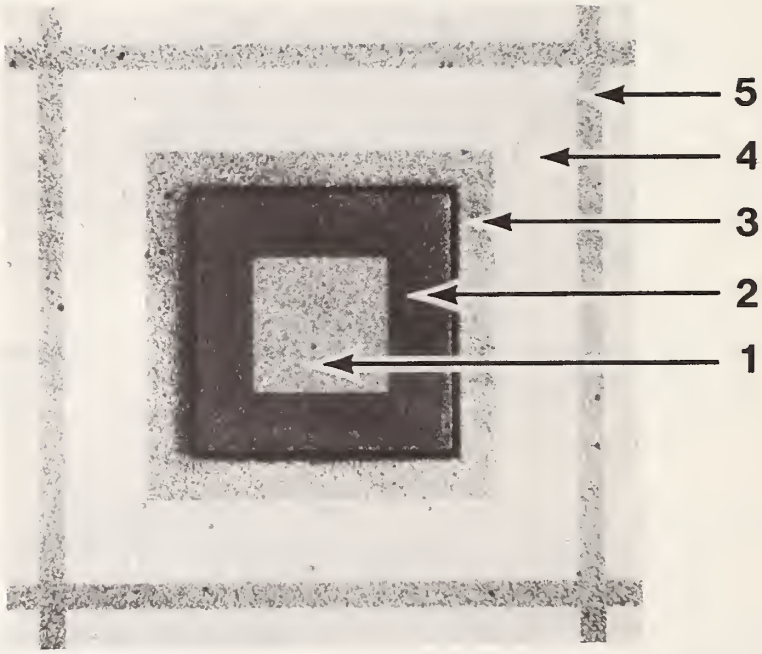


Figure 2-3. Photomicrograph of a mesa diode fabricated with test pattern NBS-20. The following areas are identified: 1) aluminum on p^+-silicon, 2) CVD oxide on p^+-silicon, 3) CVD oxide on n^--silicon, 4) aluminum on gold (0.6% Sb) on n^--silicon, and 5) cell boundaries, CVD oxide on n^--silicon.

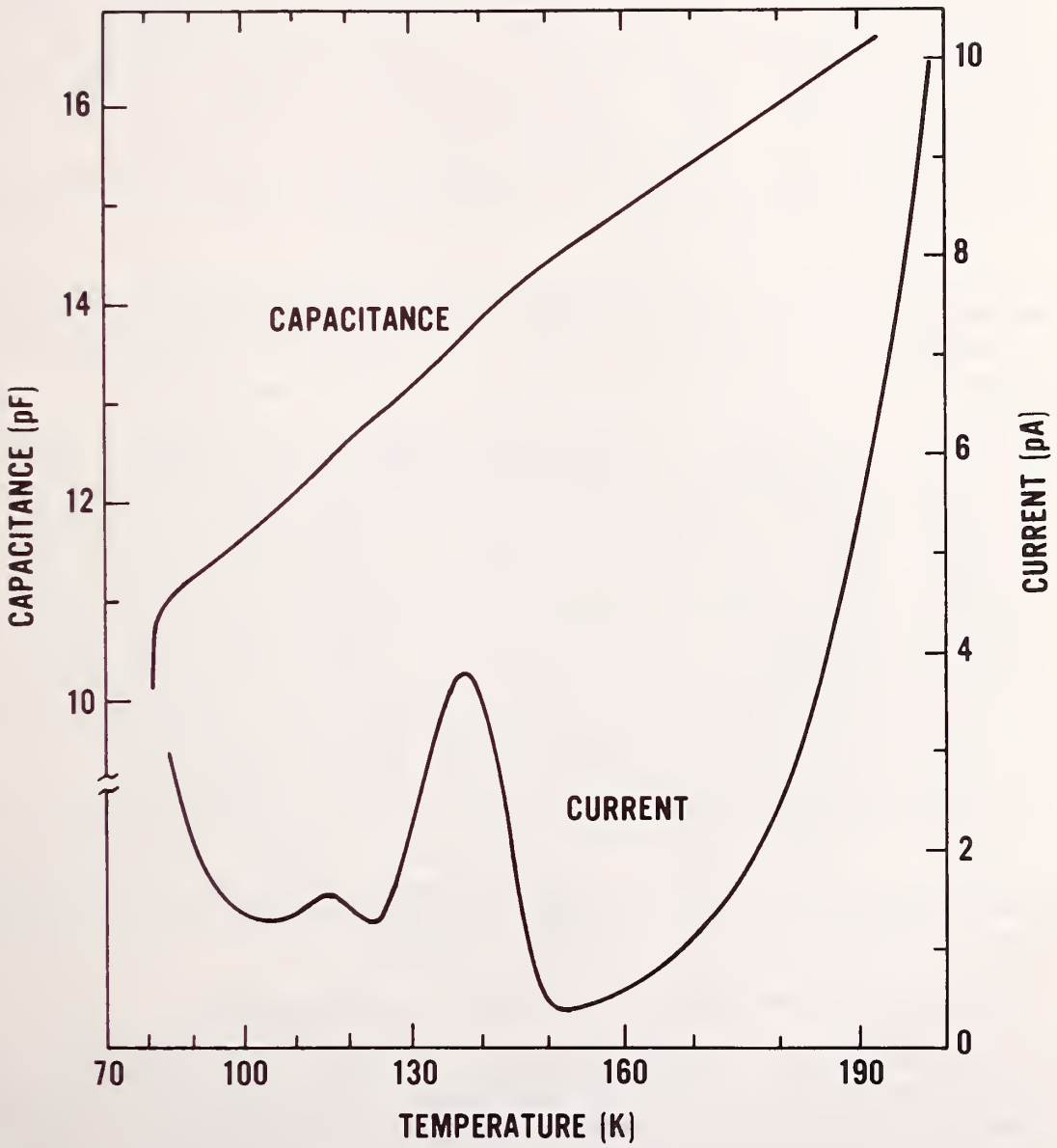


Figure 2-4. Thermally stimulated capacitance and current curves measured on a mesa diode fabricated on a $p^+n^-p^+$-wafer using test pattern NBS-20; the heating rate is about 5 K/s.

2.3.2 Deep Level Measurement Methods (Objective 2.2)

Detailed derivations and descriptions of several deep level measurement procedures were reported in the previous Annual Report [2-4, pp. 38-49], namely, 1) thermally stimulated current and capacitance measurements (TSM) which provide a quick identification of well-known defects and a measure of their density; 2) isothermal transient capacitance (ITCAP) measurements which provide a precise measurement of the combined electron and hole emission rates from the defect center over a range of temperatures and from which the energy level(s) can be determined; 3) isothermal initial and final capacitance measurements which provide a ratio of the minority-to-majority-emission rates; and 4) isothermal capacitance-leakage current measurements which provide a different combination of majority and minority emission rates, namely, the ratio of their product to their sum.

Investigation of the metrological aspects of these measurement methods and their utilization has continued with emphasis on their application to midgap defect centers which affect the operation of power devices by controlling carrier lifetime or contributing to leakage currents. Thermometry procedures were developed which improve the temperature measurement precision tenfold. This improved precision was utilized, together with an ion implantation technique developed last year [2-4, pp. 50-51], to study the sulfur midgap defect centers. Sulfur was chosen because it is a prototypical deep level having both a midgap and a shallow level and, like gold or platinum, can control the carrier lifetime. These techniques permitted the discovery of an isotope shift of sulfur in silicon. The existence of the isotope shift has significant implications for the theory of semiconductor deep levels. The four measurement procedures mentioned above were utilized to separate the majority and minority carrier emission rates for the midgap sulfur level in silicon for both ^{32}S and ^{34}S. The TSM and ITCAP procedures were also utilized for the characterization of the shallow sulfur level. Gold-doped gated silicon diodes were fabricated for use in an interlaboratory comparative study of deep-level measurement precision. A DLTS system was set up and performed as expected in measurements on gold and sulfur defect centers in silicon. These various accomplishments are described in greater detail in the following sections.

2.3.2.1 Improved Thermometry for Deep Level Measurements

The identification and characterization of impurities and defect centers in semiconductors by deep level measurement techniques such as thermally stimulated current and capacitance measurements (TSM) [2-1,2-5,2-6], deep level transient spectroscopy (DLTS) [2-2], or isothermal transient capacitance measurements (ITCAP) [2-4, pp. 40-46; 2-6] are primarily limited in their precision by thermometry. Temperature measurement procedures were developed which use carefully calibrated forward-biased temperature-sensing diodes and have a two-sigma precision ($\pm$0.02 K) that is an order of magnitude better than commercially available digital readout thermocouple systems ($\pm$0.2 K). This significant improvement in

thermometry procedures permits improved precision in the characterization of defect centers. This precision makes these deep level measurement techniques even more useful for the quick identification of defect centers necessary in an industrial environment, as well as for the more precise laboratory characterization and study of semiconductor materials.

Measurement Procedure — Two improvements were introduced to obtain the better precision of the temperature determination. First, the temperature-sensing element is placed in good thermal contact with the device under test. This is done by mounting both the temperature-sensing element and the device under test on a ceramic chip mounted on a 10-pin TO-5 header [2-1]. The ceramic is gold plated on the top and the bottom, with an isolation gap in the gold on the top forming separate areas for the temperature-sensing element and the device under test. The mounting may be by a gold eutectic or metal-impregnated epoxy. (However, it was observed that epoxy-mounted devices sometimes have extraneous TSM responses.) The TO-5 header is hermetically sealed, is coated with thermal compound, and is tightly clamped into a recess in the copper heat sink.

The second improvement is to use a forward-biased diode as the temperature-sensing device. The temperature-sensing diodes are commercially obtainable silicon diodes [2-7]. The basic parameter measured in this procedure is the voltage drop (approximately 0.35 to 1.0 V) across the diode with constant forward current. A commercial constant current generator is carefully adjusted to supply 10.000 μA by measuring the voltage drop across a low-temperature-coefficient resistor (∿100 kΩ) of known value, and the current is then switched to the temperature-sensing diode. The voltage drop is measured with a high impedance ($>10^{10}$ Ω) 5 1/2-digit voltmeter with an analog output which drives the temperature axis of an X-Y recorder for the TSM. Stability of the constant current source is very important. This system has better than 0.02-percent stability after warmup. Because of fabrication nonuniformities, each temperature-sensing diode is unique and must be individually calibrated.

Calibration — The temperature-sensing diodes are mounted in TO-5 headers as discussed above and then calibrated individually in a temperature-regulated cryostat. The TO-5 header is in good thermal contact with a high-conductivity copper heat sink in which are embedded dual Type K [2-8] thermocouples. One thermocouple is connected to a commercial temperature regulator which controls the power input to a 150-W heater which is also embedded in the copper heat sink. The other thermocouple is connected to a commercial temperature indicator which electronically compensates for the reference potential, linearizes the thermocouple output, and digitally displays the temperature with tenth-degree resolution.

The heat sink containing the TO-5 header with the temperature-sensing diode is surrounded by an evacuated stainless steel jacket. The system

is cooled by liquid nitrogen flowing through an adjustable needle valve onto the heat sink [2-1].

The system is allowed to reach temperature equilibrium at each of 15 to 25 temperatures in the temperature range to be calibrated. The digital thermocouple reading and the temperature-sensing diode voltage are recorded at each temperature. A straight line is least squares fitted to the calibration data over the range of interest. During a given ITCAP measurement, the equation of the line is used to calculate temperature from the recorded diode voltage. The temperature drift of the system, as observed on the temperature-sensing diode voltage which drifts less than 10 μV, is less than 5 mK over several (5 to 15) min. The stability of the temperature regulation system, the precision (±10 μV) with which the relatively large temperature-sensing diode forward voltage drop (∿0.5 V) can be read, and the linearity of the diode over the appropriate temperature range (Pearson's linear correlation coefficient is 0.9999996 between 205.54 and 233.08 K) make it possible to exploit statistics to achieve a precision of ±0.02 K which is a tenfold improvement in precision over the thermocouple precision of ±0.2 K.

An example of this improvement is illustrated in figure 2-5 for a typical temperature-sensing diode. The closed circles show the imprecision of the thermocouple temperatures ($\Delta T = T_{TC} - T_R$) and the open circles show the imprecision of the temperature obtained from the temperature-sensing diode ($\Delta T = T_D - T_R$) as plotted against a reference temperature, T_R, derived from the characterization values of a sulfur-implanted diode. That is, the Arrhenius emission rate equation (see eq (2) of ref. [2-1]) was solved iteratively for T from experimental values of T with $B_x = 3.77 \times 10^6$ and $\Delta E_x = 512$ meV [2-9], and the resulting values were least squares fitted to a straight line against the temperature diode voltages. The dashed horizontal lines are the two standard deviation limits on $T_D - T_R$ and correspond to a change of ±56 μV in diode voltage. The expected 5 percent of the data points (one point) lies outside these limits. The solid horizontal lines are the two standard deviation limits on $T_{TC} - T_R$ and correspond to a change of ±7 μV in thermocouple voltage. One point again lies outside these limits. The thermocouple voltage is seen to be much more subject to noise than is the temperature-sensing diode voltage, and the temperature-sensing diode has a much greater sensitivity (2784 μV/K) than the thermocouple (34 μV/K).

Applications — This improvement in thermometry has permitted a more precise measurement [2-10] of the midgap energy level of sulfur in silicon. In that measurement, the emission rate variation was three decades with a one-standard-deviation precision (±2 meV) which is even better than that of Rosier and Sah [2-11] (±4.5 meV) where measurements were made over seven decades of emission rate variation. The improved thermometry not only improved the precision of the characterization but also simplified the measurement, because a three-decade variation in emission rate can be obtained with much simpler procedures and instrumentation than a seven-decade variation.

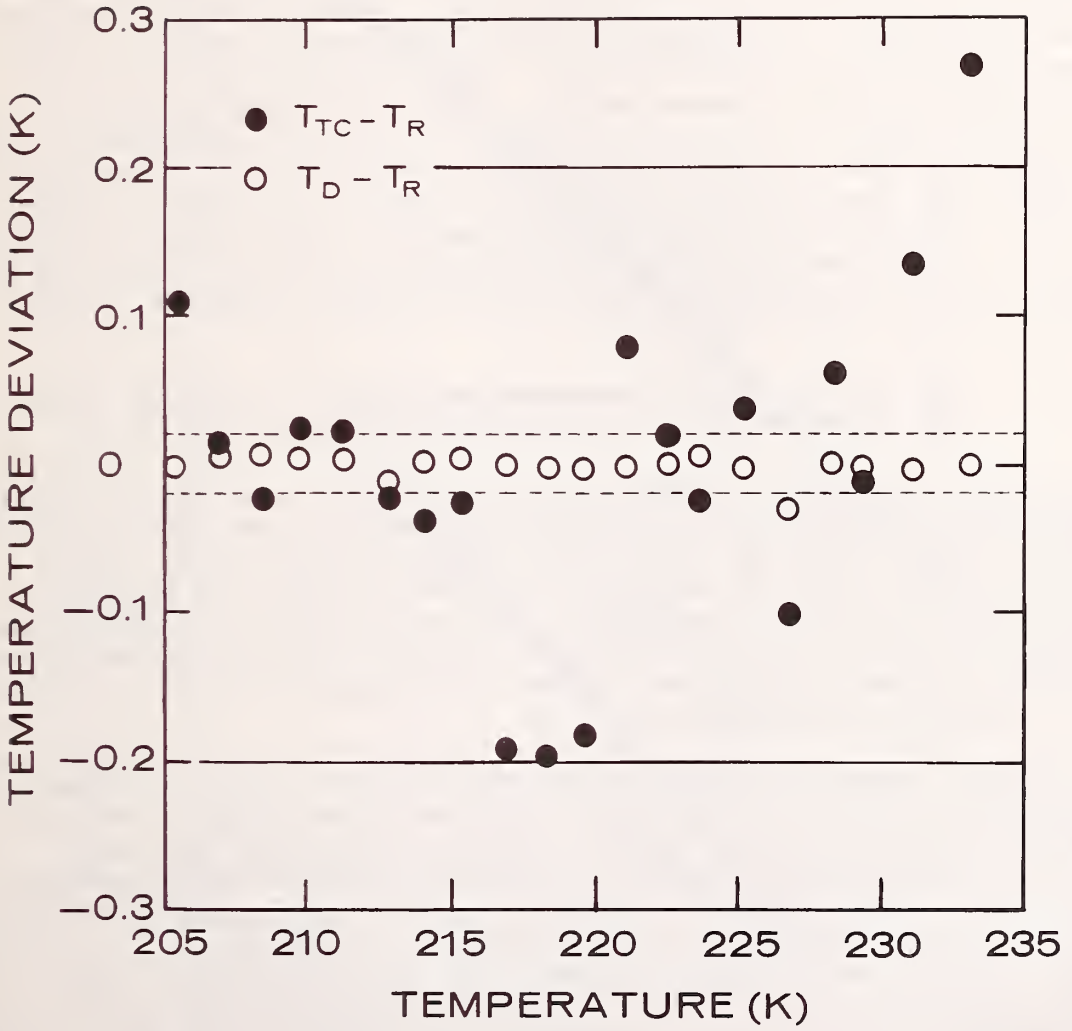


Figure 2-5. Temperature deviation of the thermocouple temperature, T_{TC}, and the temperature-sensing diode temperature, T_D, compared with a reference temperature, T_R, derived from the calculated sulfur emission rate parameters in silicon. The horizontal lines are two standard deviation limits. The solid lines and solid circles correspond to the thermocouple measurements, and the dashed line and open circles are for the diode measurements.

2.3.2.2 Use of Deep Level Measurement Techniques to Measure the Isotope Shift of Sulfur in Silicon

The characterization of the energy levels of ion-implantation-predeposited ^{32}S in silicon by TSM were previously reported [2-4, pp. 40-47; 2-10]. The midgap level is 526 $\pm$ 2 meV below the conduction band. This result is in good agreement with previous studies of the energy levels of sulfur diffused into silicon [2-11] with a midgap level of 528 $\pm$ 4.5 meV below the conduction band. Natural sulfur is 95 percent ^{32}S [2-12]. The present study was undertaken in order to evaluate the deep energy level of ^{34}S in silicon and demonstrate the precision of the measurement methods. The energy level of the ^{34}S defect was found to be 512 $\pm$ 2 meV below the conduction band edge. The existence of this isotope shift of 14 $\pm$ 4 meV in the sulfur deep level implies that these levels are strongly coupled to the lattice vibrations. Details of these results have been published [2-9]; the publication is included with this report as Appendix B. These results represent the first time that an isotope shift has been observed in a deep impurity level in silicon.

2.3.2.3 Use of Deep Level Measurement Techniques to Separate the Midgap Sulfur Majority and Minority Carrier Emission Rates

In order to evaluate the semiconductor deep level measurement techniques which were developed for the separation of majority and minority carrier emission rates [2-4, pp. 46-49], the techniques were applied to the midgap defect center of ion-implanted sulfur isotopes ^{32}S and ^{34}S in silicon. The objectives were to evaluate the ability of the procedures 1) to measure very low minority carrier emission rates and 2) to resolve the small differences between the energy levels of the isotopes. Both objectives were achieved.

Isothermal transient capacitance measurements were made at various temperatures. These measurements give the sum of the electron and hole emission rates ($e_n + e_p$). At the same time, the values for the initial and final capacitances were measured for each of the temperatures. These measurements give the ratio of hole-to-electron emission rates (e_p/e_n). The sum ($e_n + e_p$) divided by 1 + (e_p/e_n) gives e_n, and the sum minus e_n gives e_p at each temperature. Arrhenius plots of the logarithm of e_n/T^2 and e_p/T^2 against inverse temperature for each of the isotopes ^{32}S and ^{34}S are shown in figure 2-6. The open circles are ^{32}S data points and the solid circles are ^{34}S data points. The solid lines are a least squares fit to the electron emission rate data and the dashed lines, to the hole emission rate data. The activation energies are calculated as above from the slopes of the lines and the emission coefficients are calculated from the intercepts. The results are tabulated in table 2-1.

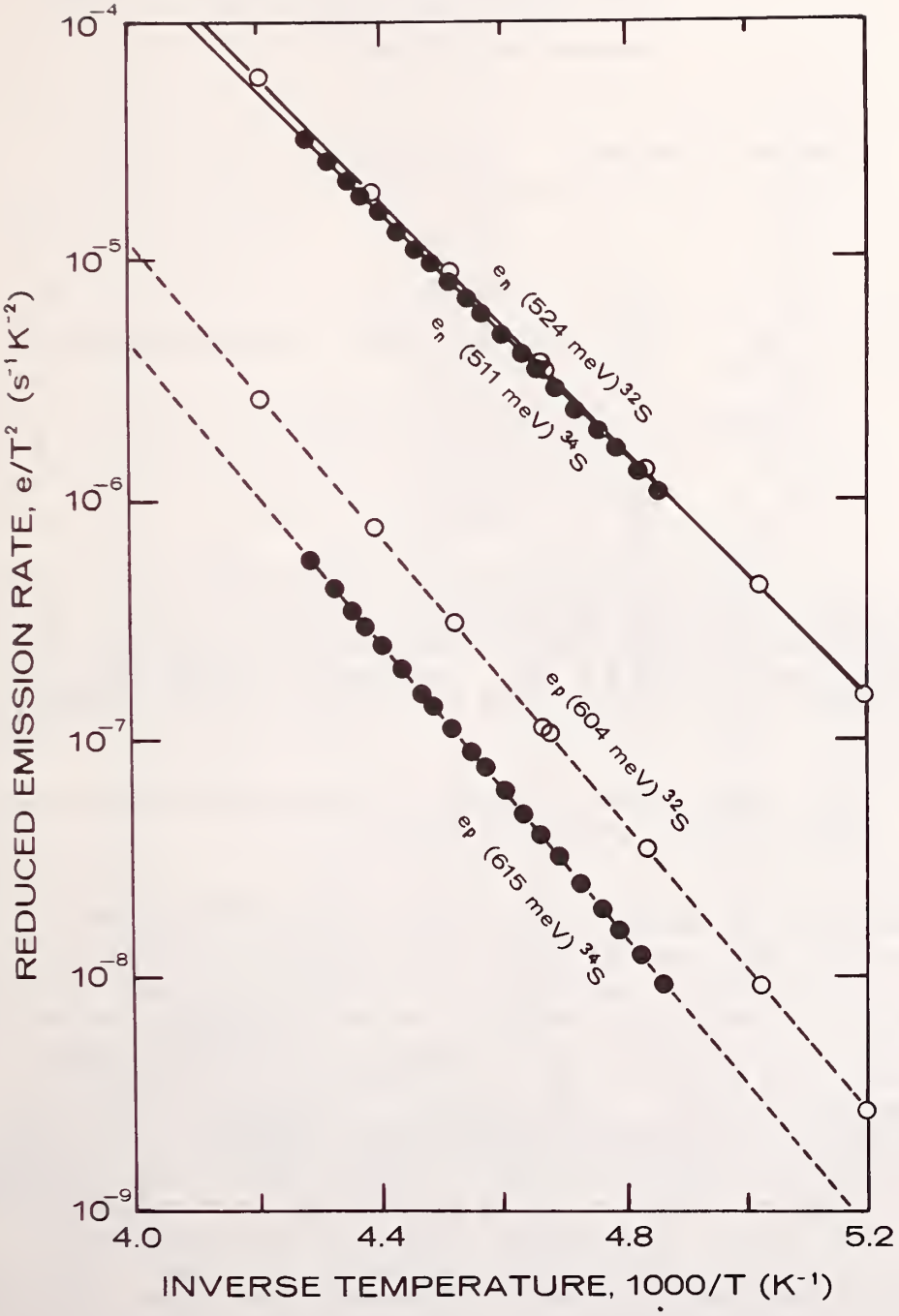


Figure 2-6. Semilog plot of reduced emission rate (e/T^2) against inverse temperature for electron (e_n) and hole (e_p) emission from the deep level centers of ^{32}S (open circles) and ^{34}S (solid circles) in silicon. Solid lines are least-squares fit to the electron emission data and dashed lines, the hole emission data.

Table 2-1. Activation Energies (ΔE_x) and Emission Coefficients (B_x) for Combined and Separated Electron and Hole Emission Rates from ^{32}S and ^{34}S Midgap Defect Centers in Silicon.

Isotope	Emission	ΔE_x (meV)	B_x ($s^{-1} K^{-2}$)
^{32}S	$e_n + e_p$	526 ± 2	$(9.3 \pm 0.5) \times 10^6$
^{32}S	e_n	524 ± 2	$(7.5 \pm 0.8) \times 10^6$
^{32}S	e_p	604 ± 3	$(1.8 \pm 0.4) \times 10^7$
^{34}S	$e_n + e_p$	512 ± 2.6	$(3.8 \pm 0.6) \times 10^6$
^{34}S	e_n	511 ± 2	$(3.5 \pm 0.6) \times 10^6$
^{34}S	e_p	615 ± 4	$(1.1 \pm 0.2) \times 10^7$

The sum of the activation energies from the defect level to the valence band ΔE_p and to the conduction band ΔE_n is 1128 ± 4 meV for ^{32}S. For ^{34}S, the sum is 1126 ± 5 meV. The sums are in satisfactory agreement with each other and with the known value of the band gap energy.

2.3.2.4 Use of Deep Level Measurement Techniques to Characterize the Shallow Sulfur Level in Silicon

Isothermal transient capacitance methods [2-4, pp. 40-46] were utilized to characterize the shallow sulfur level in both ^{32}S and ^{34}S implanted p^+n-junctions fabricated on 5 to 10 Ω·cm <111> n-type silicon as described in Appendix B. The devices were the same as used to characterize the midgap centers. The results of the evaluation of ΔE_n and B_n in the emission rate equation, $e_n = B_n T^2 \exp(-E_n/kT)$, are tabulated in table 2-2 for two representative ^{32}S implanted devices and one ^{34}S device. Hole emission is negligible for this shallow level. The indicated uncertainties represent one standard deviation in the least squares fit of a straight line to the experimental data. The larger uncertainties in the ^{34}S characterization as compared to ^{32}S are due to a smaller density of ^{34}S defect centers despite the use of a larger diode (device 19.6). These results are graphically displayed in figure 2-7. Despite the larger uncertainties in the ^{34}S characterization, it is concluded that there is no evidence of an isotope shift of the shallow sulfur level in silicon.

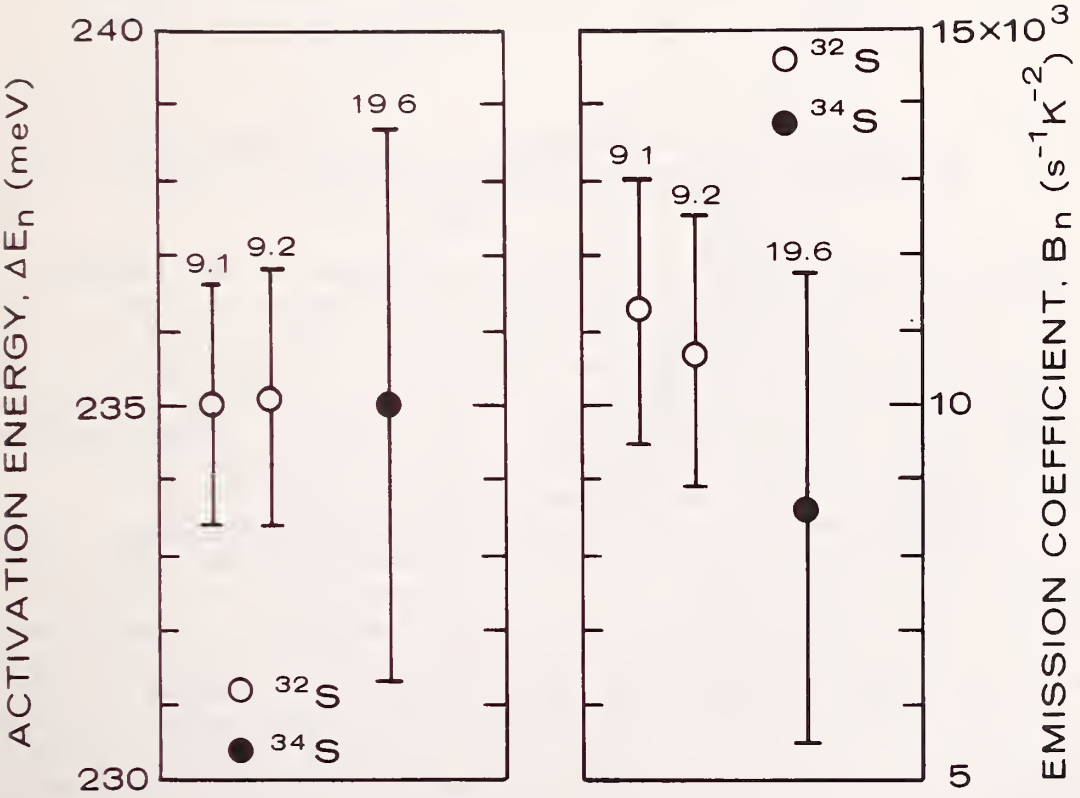


Figure 2-7. Activation energy (ΔE_n) and emission coefficient (B_n) with standard deviations for the shallow level of ^{32}S and ^{34}S in silicon.

Table 2-2. Activation Energies (ΔE_n) and Emission Coefficients (B_n) for Electron Emission from the ^{32}S and ^{34}S Shallow Level in Silicon.

Isotope	Device	ΔE_n (meV)	B_n ($s^{-1}T^{-2}$)
^{32}S	9.1	235.0 ± 1.6	11300 ± 16%
^{32}S	9.2	235.1 ± 1.7	10700 ± 17%
^{34}S	19.6	235.0 ± 3.6	8600 ± 36.7%

2.3.2.5 Use of Deep Level Measurement Techniques to Study the Variation of the Relative Density of Shallow and Deep Sulfur Defect Centers with Implantation Fluence

In order to study the effects of implantation density upon sulfur-implanted devices, ^{32}S was implanted in p^+n-junctions to a dose of 1 x 10^{13} cm^{-2} (compared to the previous dose of 2 x 10^{14} cm^{-2}). The resultant defect densities were determined from the magnitude of the dynathermal capacitance transients. It was found that the defect density associated with the shallow level is not always the same as that of the deep level. For the case of ^{32}S implanted to a dose of 2 x 10^{14} cm^{-2}, both centers were equally populated at 1.5 x 10^{13} cm^{-3}. This result is similar to that observed in previously published studies of sulfur diffused into silicon [2-11]. However, for the case of ^{32}S implanted to a dose of 1 x 10^{13} cm^{-2}, the transients for the shallow and deep centers were no longer of the same magnitude as illustrated in figure 2-8. The deeper sulfur defect appears at almost the same density as for the higher fluence implantation; however, the density of the shallow level is reduced by a factor of approximately seven. Implantation of ^{34}S to a dose of 1 x 10^{13} cm^{-2} also led to unequal transients for the shallow and deep centers. The density differences observed in the more lightly implanted devices bring into question another aspect of the theoretical treatments of the sulfur center. Pseudopotential theories of the sulfur centers based on the effective mass theory [2-13] predict that substitutional sulfur would have two energy levels within the silicon bandgap, while models of the same center based on the Slater self-consistent field method [2-14] suggest that one of the sulfur energy levels would be resonant with the silicon valence band. The fact that equal densities had been seen for the shallow and deep defect levels had been taken as implying that both these levels arose from the same center, thereby supporting the pseudopotential treatment. However, the present results suggest that the density of the center responsible for the shallow level increases with increasing sulfur implant dose,

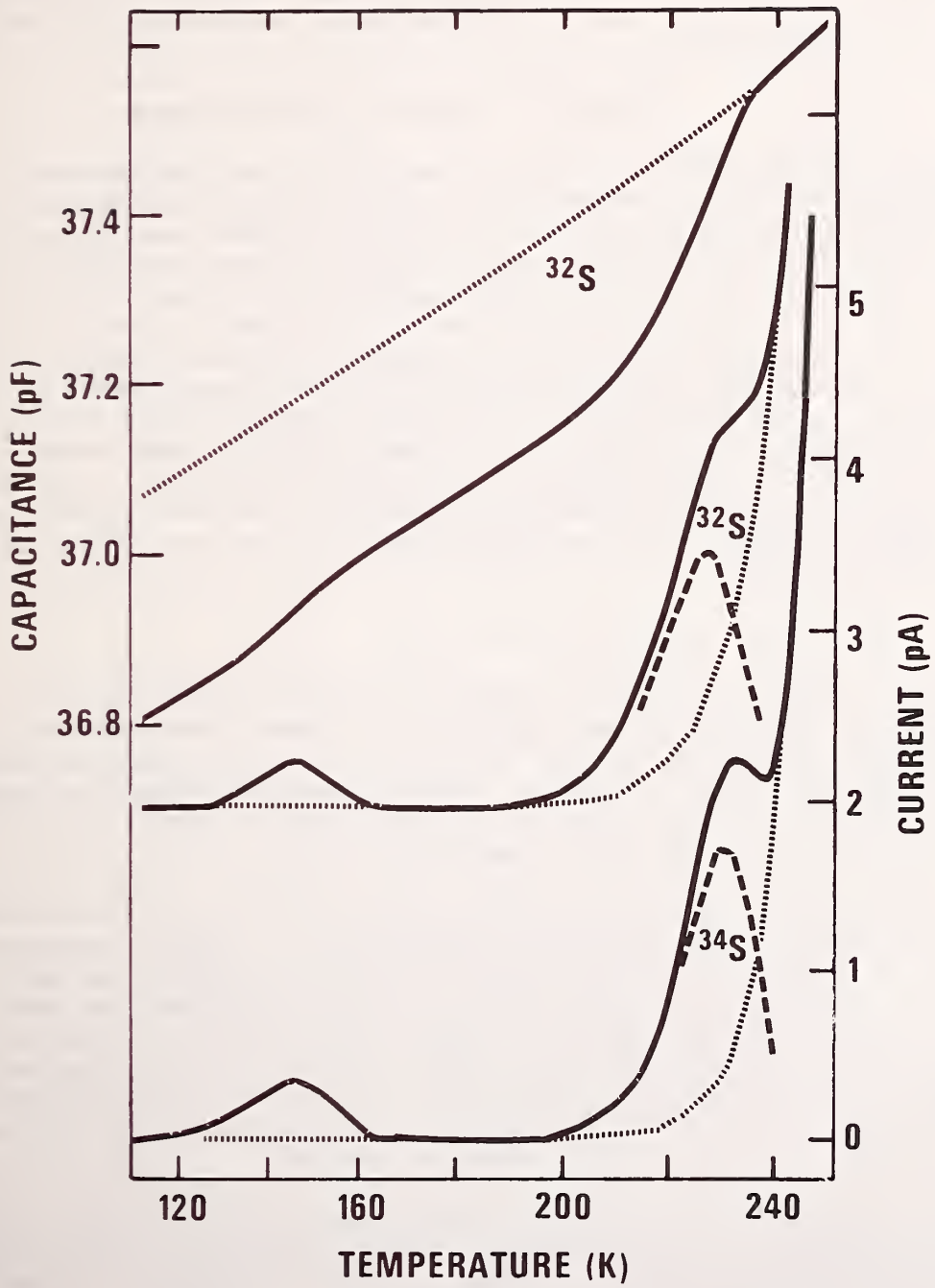


Figure 2-8. Dynathermal capacitance and current responses of a silicon p^+n-junction diode implanted with ^{32}S to a dose of 1×10^{13} cm^{-2} and the current response with ^{34}S of the same dose. The heating rate was about 10 K/s.

while the density of the center responsible for the deeper level remains nearly constant, thus weakening the support for the pseudopotential model.

This study illustrates the power of deep level measurements to answer fundamental questions related to understanding and controlling impurities in semiconductors.

2.3.2.6 Artifacts for Comparative Deep Level Measurements

A comparative study was initiated so that interested laboratories could assess their ability to measure deep level impurities accurately. In this study, a pair of gold-doped silicon gated diodes was made available for measurement of defect energy levels and associated densities and emission rates by each interested laboratory. At the completion of this study, a listing of all the values obtained and the methods used by the participating laboratories will be made available. However, the names of the participating laboratories will not be associated with their data in this compilation. It is hoped that this type of interlaboratory comparison will raise the general level of competence in the field of deep level measurements to a point that they will become more effectively and widely used by the semiconductor industry. It is anticipated that at least three laboratories will participate in this study by the end of FY 79.

2.3.2.7 Deep Level Transient Spectroscopy

The primary method used by this laboratory for the detection and characterization of deep levels have been the isothermal transient capacitance (ITCAP) technique and the thermally stimulated current and capacitance measurement (TSM) technique. These methods have been discussed in earlier reports [2-4, pp. 38-46; 2-15, pp. 74-87] and applied in the previous sections to the case of implanted sulfur.

In the ITCAP method, the device under test is held at a fixed temperature; the change in the depletion capacitance due to defect emission is recorded as a function of time after the defect is charged by the application of a momentary zero-bias pulse. In the TSM techniques, the device is cooled below the emission temperature of the defect and the defects are then charged; emission is then allowed by heating the device at some known heating rate. Effectively, both of these measurements occur at dc since the defects are charged once, and the emission response to the single charging event is directly recorded.

Another technique described in the last annual report [2-4, pp. 51-59] is an extension of the ITCAP method. Rather than recording the response to a single charging pulse as is done in ITCAP, charging pulses are applied to the device at regular intervals to allow a periodic repetition of charging and emission. This method transforms the measurement from

dc to the repetition frequency of the pulses and allows alternative methods for signal processing. In this case, a minicomputer system was utilized to capture, digitize, and analyze the capacitance transient.

Another deep level measurement technique which is rapidly gaining popularity is the deep level transient spectroscopy (DLTS) method [2-2]. In principle, this method is the same as the extended ITCAP technique, but there are two basic differences in implementation. First, the capacitance measurements are made at higher frequencies (10 to 50 MHz), and, second, the technique utilizes a dual-channel box-car integrator for the signal processing. The attractive attributes of this method are the spectroscopic nature of the recorded data and the relative ease with which energy levels can be deduced. (However, as is true for all of the described methods, the accuracy of the results is dependent on the care exercised with the thermometry [see sec. 2.3.2.1].)

Because of the prevalence of the users of DLTS, an apparatus of this type was set up in this laboratory to allow direct comparison to existing methods. The apparatus is similar in nature to that described by Lang [2-16]. It basically consists of a high frequency capacitance bridge and the dual-channel box-car integrator system. To date, preliminary DLTS measurements have been made on the midgap gold acceptor, the shallow gold donor, and the midgap sulfur level; the energy levels determined agreed with previous measurements by the ITCAP method within experimental uncertainties.

2.3.3 Correlation of Defects with Device Parameters (Objective 2.3)

The bulk deep level defects in high power devices are already present in the starting material or are introduced either intentionally or unintentionally during wafer processing. In order to realize specific electrical characteristics of their devices, manufacturers must be able to control their processes to minimize unwanted defects and to optimize the nature and number of defects [2-17] which are used to control the lifetime of minority carriers [2-18] or switching characteristics of devices. Another aspect of the introduction of specific defects to control lifetime is the ability to fabricate wafers with controlled characteristics over the full area of the wafer. This is important, for example, in a thyristor's ability to switch without developing hot spots. In addition to lifetime, the influence of deep level defects on such electrical parameters as junction forward voltage drop and reverse leakage current must be well-characterized.

The hot/cold wafer-probing apparatus [2-19,2-20] was used to map the two-dimensional spatial variation of deep level defects across a gold-diffused wafer. It was also used to map the diode reverse leakage and the forward voltage drop. Similar electrical measurements were made on commercially fabricated power rectifiers in wafer form; in addition,

a direct comparison of the diode reverse recovery lifetime and the open circuit voltage decay (OCVD) lifetime was made.

2.3.3.1 Reverse Leakage Current and Forward Voltage Drop of Diodes

Reverse leakage current in *pn*-junctions can originate from at least three sources: 1) generation in the depletion layer, 2) diffusion of minority carriers into the depletion layer, and 3) conduction along the surface layer. In general, surface leakage is a consequence of surface contamination due to improper processing or a consequence of improper device design to minimize surface fields. At room temperature, leakage by diffusion of minority carriers into depletion regions is negligible for silicon devices. Hence, under most circumstances, the reverse leakage current is dominated by carrier generation in the depletion layer. Some qualitative estimates of the behavior of devices with such factors as lifetime, diffusion length, injection level, and forward voltage can be seen from an examination of the basic diode equations.

The generation leakage current, I_{GEN}, is proportional to the carrier generation rate per unit volume, U, and the volume of the depletion region. Thus:

$$I_{GEN} = q\,|U|\,WA\ , \tag{2-1}$$

where q is the electronic charge and W and A are, respectively, the width and area of the depletion volume. The generation rate is given by [2-21]:

$$|U| = \frac{N_i}{2\tau_0} \tag{2-2}$$

where

$$\tau_0 \equiv \frac{\sigma n \varepsilon^{(E_t - E_i)/kT} + \sigma p \varepsilon^{(E_i - E_t)/kT}}{2\sigma_p \sigma_n v_{th} N_t}\ . \tag{2-3}$$

N_i is the intrinsic carrier density, σ_n and σ_p are the electron and hole capture cross sections, respectively, E_i is the intrinsic Fermi energy, v_{th} is the thermal velocity of carriers, and N_t is the density of recombination-generation carriers at energy E_t in the gap. The generation rate is seen to be inversely proportional to τ_0, which is the space charge generation lifetime, and directly proportional to the density of the recombination-generation centers. From the standpoint of space charge generation, devices of low reverse leakage characteristics require a long space charge generation lifetime and a small density of deep level defect centers.

Under forward bias conditions, the effect of the defect density is seen most directly at low level injection. When the injection level is very

low, recombination of carriers occurs primarily in the depletion volume through the presence of the deep level defects. The forward recombination current, I_{LL}, is then given by [2-22]:

$$I_{LL} = \frac{qN_i WA}{2\tau_0} (\varepsilon^{qV/2kT} - 1) \quad . \tag{2-4}$$

V is the forward voltage drop across the diode; simplifying assumptions entering this result include $\sigma_p = \sigma_n$ and $E_t = E_i$ in eq (2-3). It is evident from eq (2-4) that for a given low level injection current, devices with large τ_0 (i.e., low N_t) also have large forward voltage drop.

Typical high power devices operate in the high injection regime. Efficient operation under these conditions requires high forward current with low forward voltage drop. At high injection, the voltage across the lightly doped n-region of a typical diode structure is given by [2-23]:

$$V_n \approx \frac{2kT}{q} \left(\frac{d}{L_a}\right)^2 , \tag{2-5}$$

where d is the half-width of the n-region and L_a is the ambipolar diffusion length. Large values of L_a (resulting from long high level lifetime) are necessary for low forward drop in this region.

Wafer map measurements of reverse leakage current and forward voltage drop were made at room temperature on two fabricated wafers to observe the correlations indicated by eqs (2-3) and (2-4). One wafer was a gold-diffused wafer fabricated in our facilities. The tested structure was a 430-μm diameter gated diode (device number 10 of test pattern NBS-3 [2-24]) spaced at 5.08-mm intervals on the wafer. After fabrication of the p^+n-structure by diffusion of boron (3.0 μm) into <111> 5 to 10 Ω·cm n-type silicon, gold was diffused into the wafer from a back-surface-evaporated layer by a 24-h, 800°C heat treatment. The other wafer was a commercially fabricated rectifier wafer consisting of an array of 2.54-mm devices spaced on a 3.43-mm grid. The devices were p^+nn^+-structures rated at 16 A.

The reverse leakage measurements were made with a digital electrometer with an applied reverse bias of 15 V. The gates on the gold-diffused devices were biased to minimize the surface leakage; the rectifiers did not have gates.

The forward voltage drop measurements (low injection) were made under computer control. A schematic is shown in figure 2-9. A digital voltmeter (DVM) measures the voltage across the diode which has a constant current I (10 μA) through it. Switch S_1 is actually the probe which contacts the device. In a typical sequence, switch S_2 is closed to

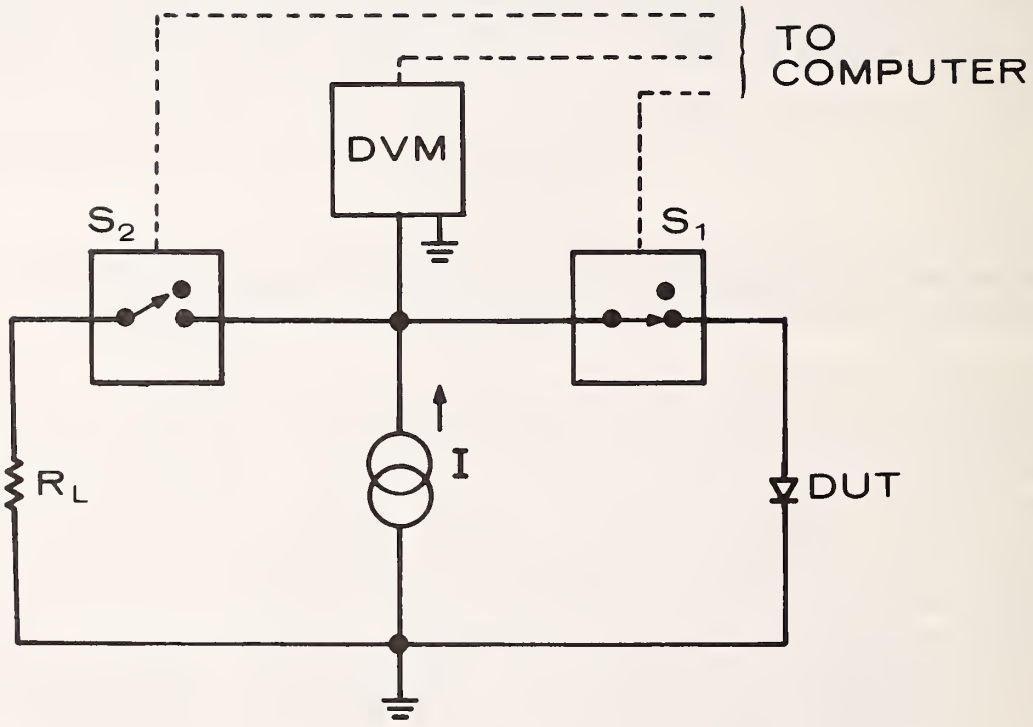


Figure 2-9. Schematic diagram of method used to measure forward voltage drop of diodes.

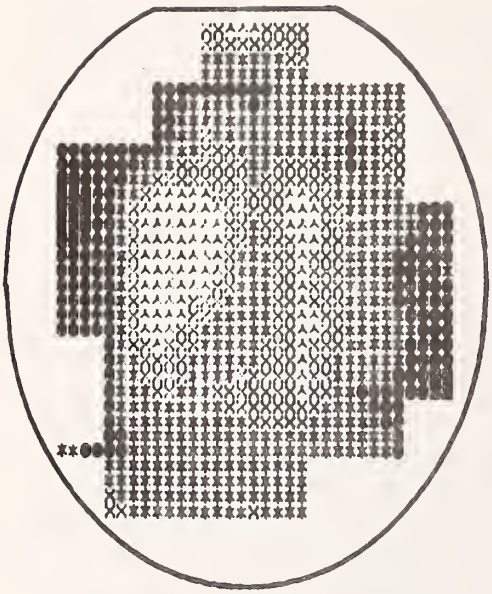
divert the current through R_L (to allow a measurement of the current and to prevent compliance limiting); then S_1 is opened and the prober is instructed to move to the next device. After reaching the next device, the device is probed (i.e., close S_1), switch S_2 is opened, and then the DVM is instructed to read. Measurements can be made at the rate of about one per second.

Figure 2-10 displays wafer maps of the gold acceptor defect density, the reverse leakage current (at 15 V), and the forward voltage drop (at 10 μA) for the gold-diffused wafer. (The lighter areas represent the smaller values of the parameter.) There is a factor of four variation in the defect density and the reverse leakage current; as seen from the patterning of the maps, regions of low defect density result in low leakage current as indicated by eqs (2-2) through (2-4). The forward voltage drop map shows similar patterning but is inversely related to the reverse leakage and the defect density maps. As indicated by eq (2-4), for a given low level current, devices with long lifetime have large forward voltage; hence, regions of low defect density (i.e., long lifetime) on the wafer correspond to regions of high forward voltage drop.

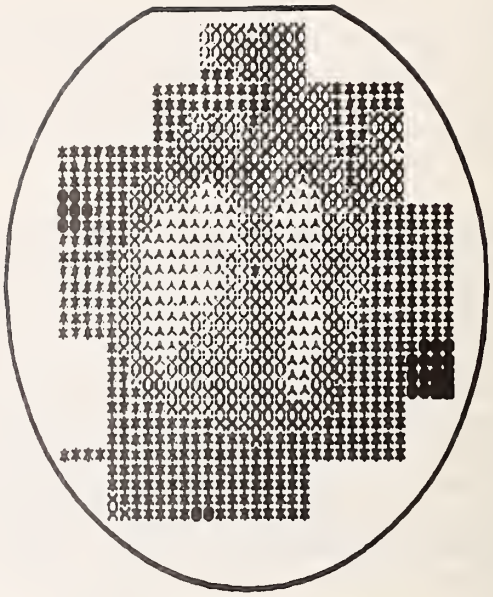
Figure 2-11 compares the forward voltage drop (at 10 μA) and the reverse leakage current (at 15 V) of the commercial rectifier wafer. As was observed in the gold-diffused wafer, these parameters have an inverse relationship on the wafer maps. Although no guard gate is available to control surface leakage on these devices, the general correspondence of the maps would indicate that generation current in the depletion region dominates the reverse leakage. Note that there is a very wide variation in the reverse leakage current. Although the wafer map for defect density for this wafer has not yet been measured, one can infer from the results on the gold-diffused wafer discussed above that the same variation exists in the density of the midgap defect center which controls the leakage. Confirming measurements of the defect density are planned for the future.

2.3.3.2 Measurement of Minority Carrier Lifetime

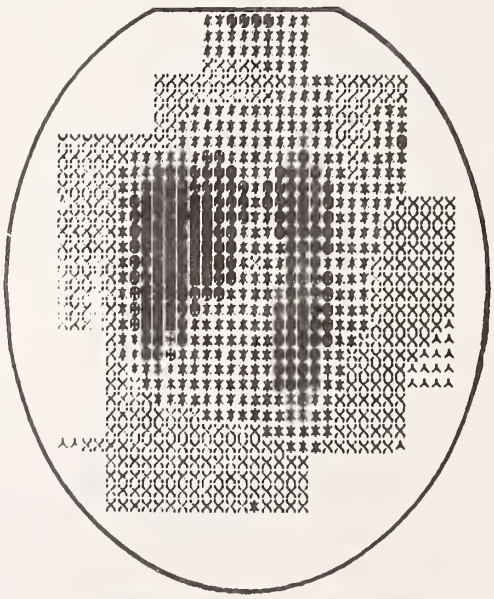
It is evident even from relatively simple considerations that lifetime of minority carriers plays an important part in the performance of semiconductor devices. The presence of deep levels in the device strongly affects the minority carrier lifetime. As seen earlier, greater density of deep levels in the depletion region results in higher reverse leakage current. The design of high power thyristors generally requires short lifetime in order to improve the recovery characteristics; however, too large a density of deep levels can also result in degradation of forward conduction characteristics. Hence, the minority carrier lifetime must be tailored to meet the specific design requirements of the devices.



GOLD ACCEPTOR DEFECT
DENSITY 1.9-7.6×10^{13} cm^{-3}



REVERSE LEAKAGE CURRENT
0.26-1.05 nA



FORWARD VOLTAGE DROP
0.42-0.46 V

Figure 2-10. Wafer maps of the gold acceptor defect density, the reverse leakage current, and the forward voltage drop for the gold-diffused wafer. (The lighter areas represent the smaller values of the parameter.)

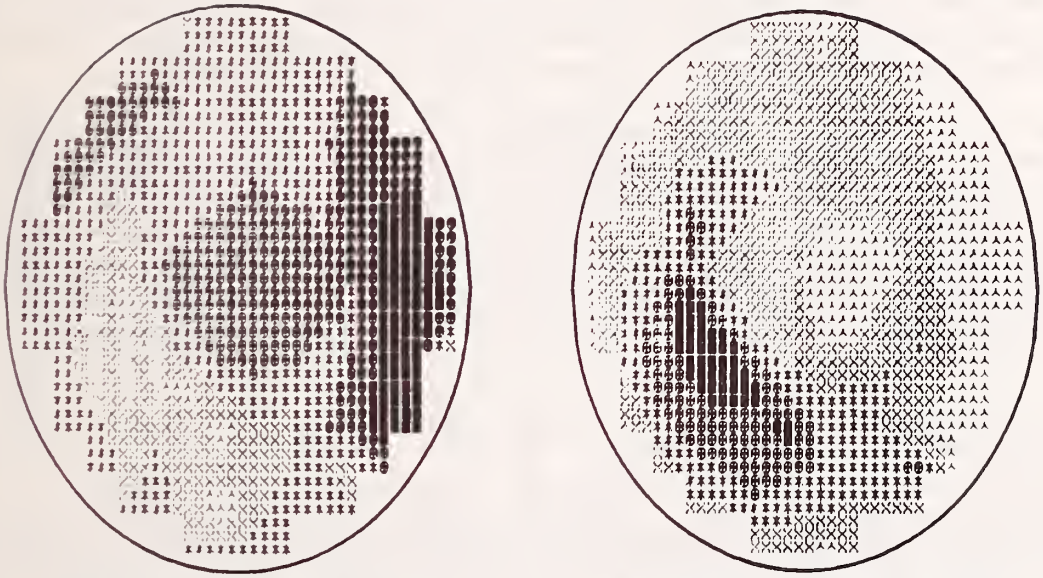


Figure 2-11. Wafer maps of the reverse leakage current and the forward voltage drop for the commercial rectifier wafer.

Two techniques for measuring minority carrier lifetime include the open circuit voltage decay (OCVD) and the diode reverse recovery methods. These two methods were implemented in order to correlate the lifetimes with the other measured electrical parameters and also to correlate the results of the two different lifetime measurements.

The OCVD lifetime is determined from the slope of the decaying forward voltage on a diode following the abrupt termination of the forward injection current. Consider the p^+nn^+-structure of a typical rectifier. Under conditions of high level injection in the lightly doped n-region, the steady-state electron and hole concentrations greatly exceed the equilibrium donor concentration, and charge neutrality causes the electron and hole concentration to be equal [2-25]. When the current is suddenly terminated, the excess carriers cause an open circuit voltage across the p^+n- and the nn^+-junctions; this excess concentration decreases in time by recombination, and hence the open circuit voltage decays with time.

Figure 2-12 shows a typical oscilloscope trace of an OCVD response of one of the devices on the commercially fabricated rectifier wafer discussed earlier. The measurements were made with a commercially available OCVD instrument.* This instrument provides a repetitive series of voltage pulses which result in alternating forward injection and open circuit on the diode. The effective high level lifetime is determined from the slope of the linear portion of the decaying voltage [2-26]

$$\tau_{HL} = - \left(\frac{2kT}{q}\right) \left(\frac{dV}{dt}\right)^{-1} . \qquad (2\text{-}6)$$

For the diode reverse recovery method, the diode is first placed in a steady-state forward bias condition as in the case of the OCVD method. But, rather than terminating the device into an open circuit as in OCVD, the voltage across the diode is abruptly reversed. At this instant, there is an abrupt reversal of current which is limited only by the external circuit; this reverse current persists as the excess carriers leave the lightly doped region (i.e., the n-region of a p^+nn^+-structure) by diffusion. At some time, t_r, after reversal of the voltage, depletion begins at the p^+n-junction and the device then begins to sustain a reverse voltage. At this point, the reverse current begins to decay toward the steady-state reverse leakage value. The minority carrier lifetime, τ, is related to the recovery time t_r by the following relationship [2-27]:

$$\text{erf}\,[t_r/\tau]^{1/2} = (1 + I_r/I_f)^{-1} . \qquad (2\text{-}7)$$

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*Solid State Measurements, Inc., Monroeville, PA, Model OCD-2.

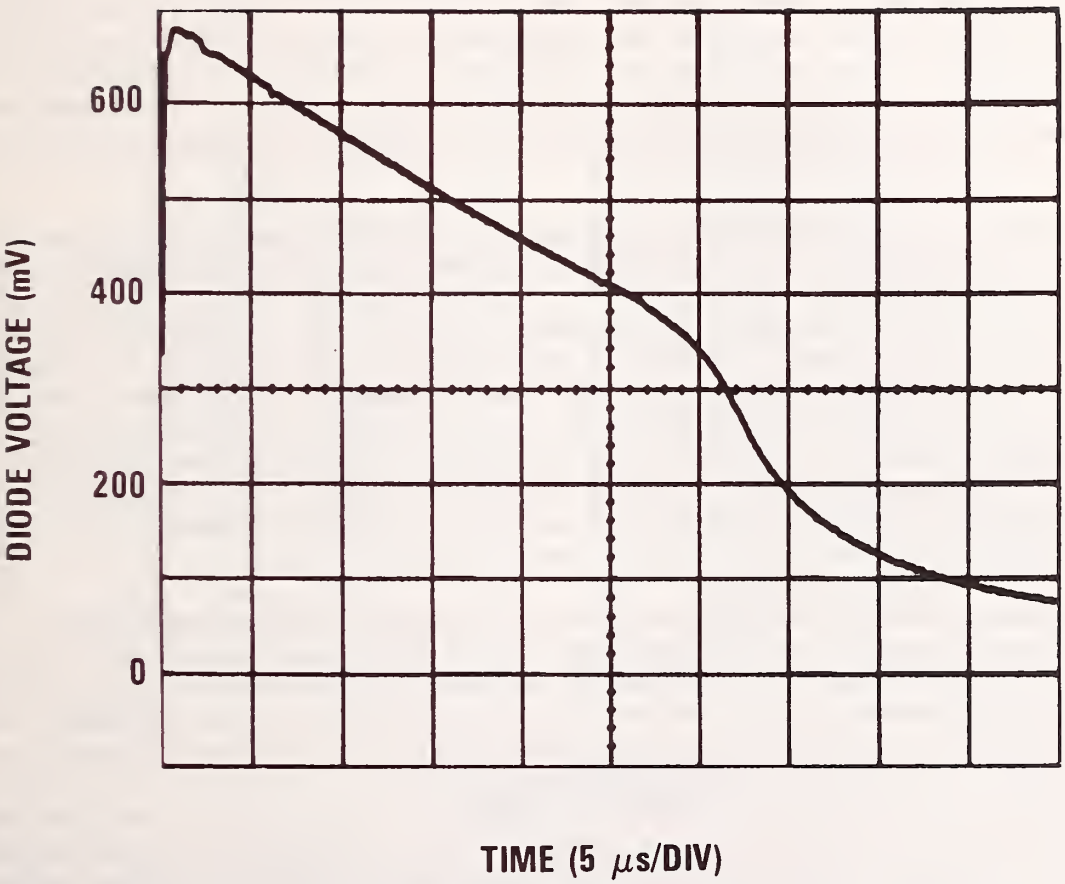

Figure 2-12. An OCVD response of a typical power rectifier diode. The high level lifetime is given by the slope of the linear portion of the high voltage region of the curve (τ_{HL} = 4.7 μs).

I_r and I_f are the magnitudes of the reverse and forward currents; for the case when $I_r = I_f$, $\tau \approx 4\ t_r$. Figure 2-13 displays an oscilloscope trace of a diode reverse recovery characteristic with $I_r = I_f$; the recovery time is shown on the figure. This is a characteristic which is typical of devices on the commercial rectifier wafer discussed previously.

Figure 2-14 shows a simplified schematic diagram of the measurement circuit for this technique. The measurements are done on the devices in wafer form. Switch S_1, as discussed previously, is the probe contact of the automatic wafer prober. The positive and negative levels of the high speed pulse generator are adjusted to give the same forward and instantaneous reverse currents. A digital oscilloscope samples and records this current transient across the load resistor. The computer is used to control the wafer prober and to analyze the transient to determine t_r and to calculate τ.

Wafer maps of the minority carrier lifetime were made on the commercial rectifier wafer using both OCVD and reverse recovery techniques. The results are shown in figure 2-15. In both cases, there is a central region of long lifetime with a crescent-shaped low lifetime region bounding it in the lower left area. The similar shading patterns indicate that the lifetimes measured by the two techniques are proportional; however, the absolute magnitudes are seen to differ by a significant amount. Note, in addition, the correlation between these lifetime maps and the forward voltage drop and leakage current maps (fig. 2-11). In particular, it is observed that in regions of high leakage (i.e., high density of generation centers) the lifetime is low.

Finally, compared in figure 2-16 are the OCVD lifetime wafer maps of two separate wafers. These are commercially fabricated wafers with identical part numbers and, presumably, satisfy some common set of electrical specifications. Yet it is evident from the figure that they have vastly different open circuit voltage decay lifetimes. In the left wafer of figure 2-16, the OCVD lifetimes range from 1.7 to 5.2 μs, with 50 percent of the devices falling in the range 3.1 to 3.8 μs. The other wafer has a range of 4.9 to 9.4 μs, with half the devices falling in the range 7.6 to 8.5 μs. The total variation of OCVD lifetime for these two wafers is 1.7 to 9.4 μs, with only a very small region of overlap between the two wafers (14 devices total in the range 4.5 to 5.8 μs, or 5 percent). These results would suggest that there are variations in processing procedures or starting material characteristics which may prevent tighter control of electrical device specifications.

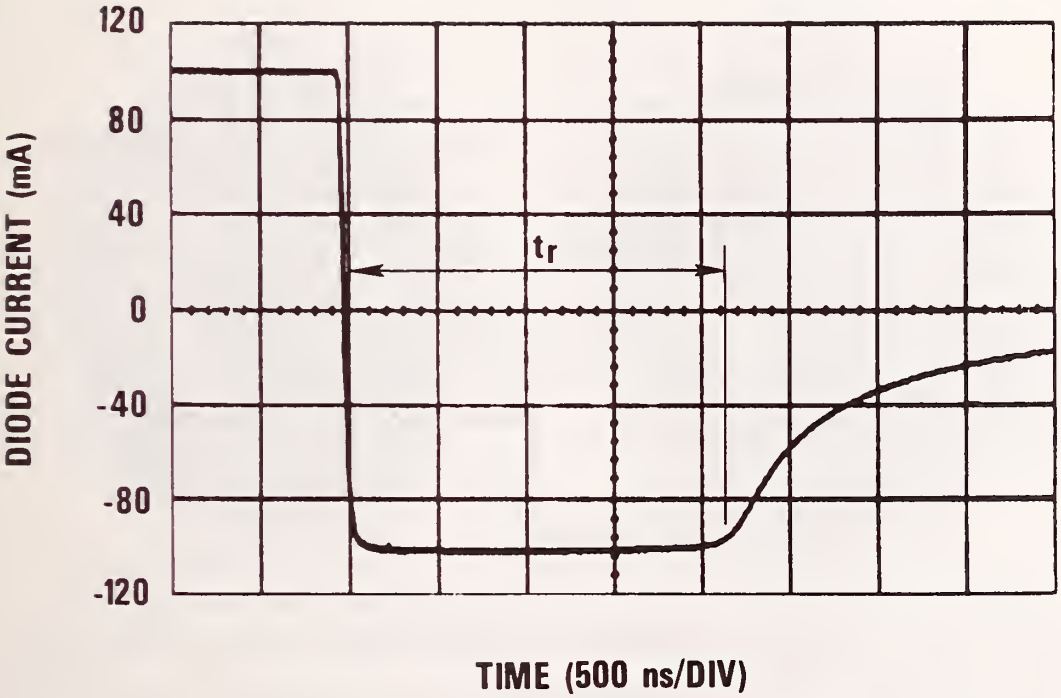

Figure 2-13. The diode reverse recovery characteristic of a typical power rectifier diode. The defined recovery time is indicated.

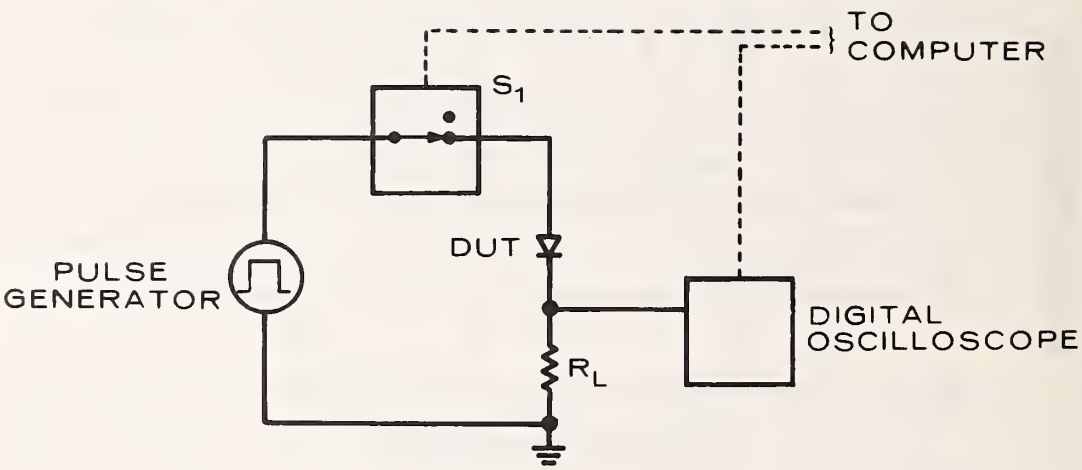

Figure 2-14. Schematic diagram of method used to measure the diode reverse recovery time.

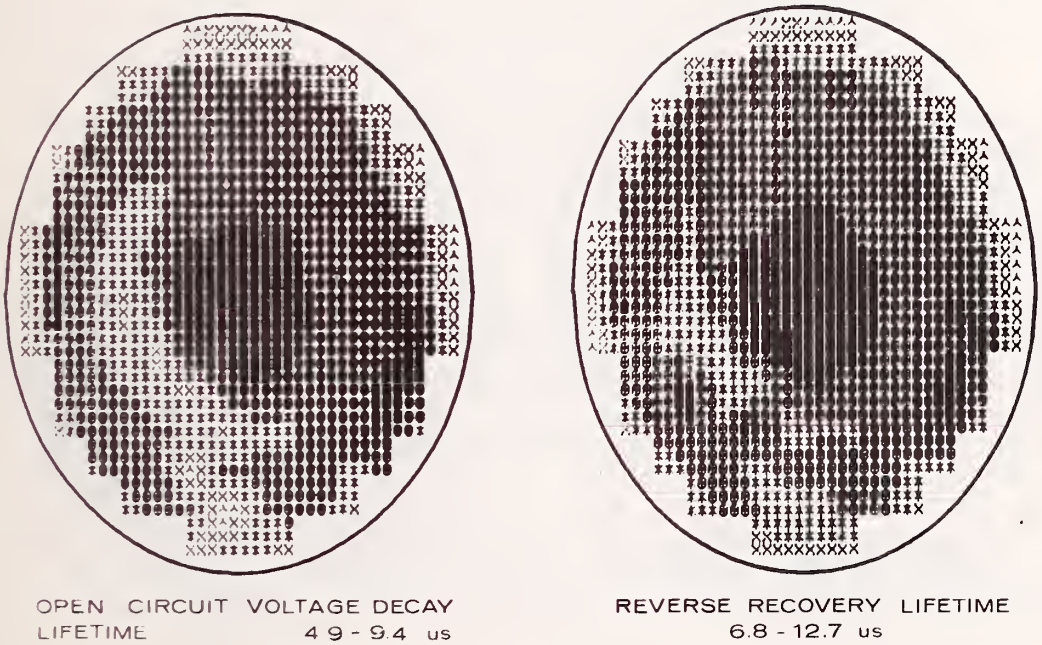

Figure 2-15. Wafer maps of the minority carrier lifetime of the commercial rectifier wafer determined by the open circuit voltage decay and reverse recovery techniques. In each case, regions of short lifetimes correspond to the light areas.

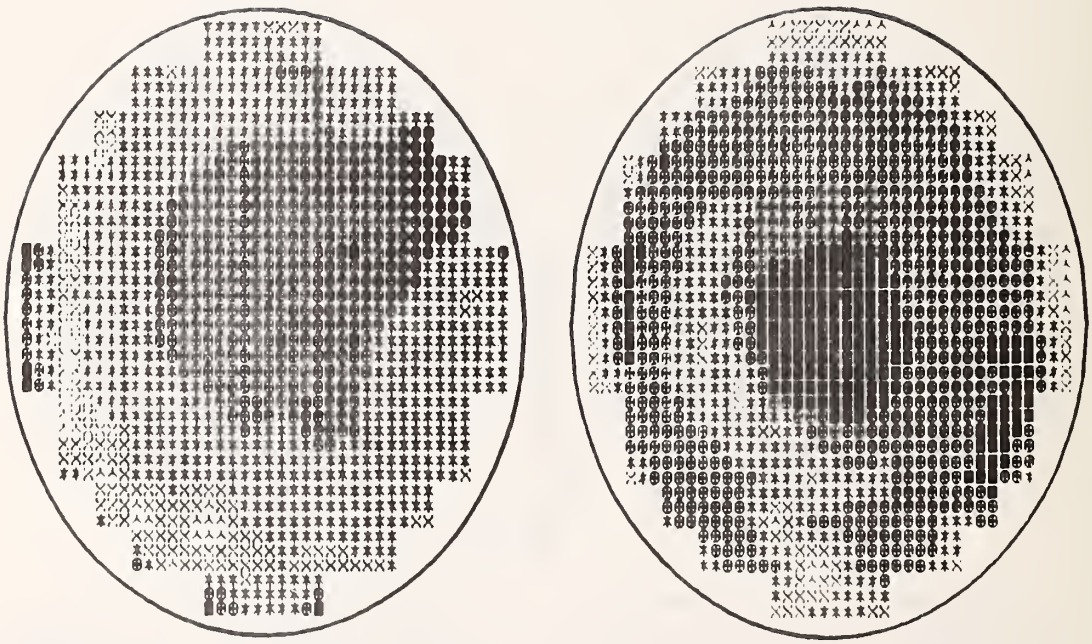

Figure 2-16. Wafer maps of OCVD lifetime of two similar commercially fabricated wafers. The range of lifetime in the left wafer is 1.7 to 5.2 μs; that of the right wafer is 4.9 to 9.4 μs.

3. SPREADING RESISTANCE MEASUREMENTS

by

J. R. Ehrstein, D. R. Ricks, and L. A. Robinson

3.1 Objectives

The overall objective of this task, which began in October 1977, is to increase the reliability with which spreading resistance measurements can be used for radial resistivity screening of thyristor substrate material and for depth resistivity profiling of partially or fully fabricated thyristor structures. The end use for such measurements extends from process control during thyristor fabrication to profile analysis required for design and performance modeling of newer or more advanced thyristor structures. The specific objectives are as follows:

3.1 Develop a silicon surface preparation procedure which enables stable and reproducible spreading resistance measurements to be obtained on bulk (111) n-type silicon in the resistivity range (20 to 400 Ω·cm) which covers thyristor substrate material.

3.2 Based on the foregoing, develop a surface preparation procedure for bevel sectioning of thyristor structures which yields improved data quality in the n-base layer compared with presently obtainable results, while retaining the favorable data character presently obtainable in other regions of the sectioned thyristor.

3.3 Conduct a preliminary test of the equivalence of boron-, gallium-, and aluminum-doped silicon specimens for the calibration of spreading resistance measurements of p-type thyristor diffusions.

This report discusses the progress that has been made in each of these areas during FY 1978.

3.2 Background

The ability to measure and to control dopant profiles is important in thyristor structures for a variety of reasons. The state of lateral uniformity of dopant in the high resistivity n-type silicon, which later forms the thyristor n-base region, determines the reverse blocking voltage which can be achieved. Blocking voltage must be designed around the lowest local resistivity value expected in the n-base starting material. Other thyristor parameters are controlled or strongly influenced by dopant profiles: 1) the contact resistance between the thyristor structure and the metallization is affected by the electrically active dopant at the surface of the emitter layers and 2) the on-state injection effici-

ency is affected by the dopant profile in the vicinity of the junction between the cathode emitter and p-base.

The spreading resistance technique is well-suited to measuring the resistivity variations in the high resistivity n-type silicon which is used for the thyristor n-base, as well as to measuring the resistivity variations in depth resulting from the n- and p-type dopant diffusions used to fabricate a thyristor. This technique generally utilizes two hardened alloy probes with small tip radius. The tips are closely spaced, on the order of 100 μm and are carefully lowered to the semiconductor surface. A voltage is applied across the probes, and the resulting current, which is related to the resistivity of the specimen where it contacts the probes, is measured. The ratio of applied voltage to resulting current is taken to be the spreading resistance, R_{SP}. The probes are then lifted and advanced a selected distance, and the measurement process is repeated. The resulting array of measurements can then be related to the resistivity at each position on the specimen. Specimens are typically prepared for top surface measurement by mechanical lapping or by mechanical or chem-mechanical polishing of the surface to be measured. For depth profiling, a small section is cut from the finished device and mounted on a block whose face has been ground at a small angle to the horizontal. This block is then attached to a piston in a collar, as shown in figure 3-1, for sectioning of the specimen. The sectioning is accomplished using a mechanical or chem-mechanical process, as above. When the specimen and mounting block are transferred to the spreading resistance measurement stage, lateral step advance of the probes corresponds to measurement at increasing depth in the specimen, as represented in figure 3-2. The proceedings of a 1974 symposium provide a number of useful articles on the subject of spreading resistance measurements [3-1].

In addition to having high spatial resolution for both lateral and depth profiling, spreading resistance has the large dynamic range of measurable resistivity values required for depth profiling of graded layers in thyristor or other semiconductor structures. It is, however, a comparative technique: resistivity values can be derived from spreading resistance values only after the apparatus has been calibrated against specimens of known resistivity. This calibration is known to depend upon the conductivity type and crystallographic orientation of the specimens, on the surface preparation given the specimens, and possibly upon the dopant species [3-2]. Further, to derive resistivity values when measurements are made on specimens with vertically graded resistivity, as in diffused layers, a mathematical algorithm is required [3-3,3-4,3-5].

Nevertheless, spreading resistance offers the capability of process control on a routine basis if measurements are reliable and repeatable and if costs and turnaround times are acceptable. It also offers the design or process engineer the possibility of data feedback regarding the profiles obtained by new or modified process cycles. Information of this type should aid in the achievement of very high blocking voltage devices envisioned for high voltage dc transmission systems.

Figure 3-1. Silicon chip mounted on beveling block with piston and collar used in beveling procedure.

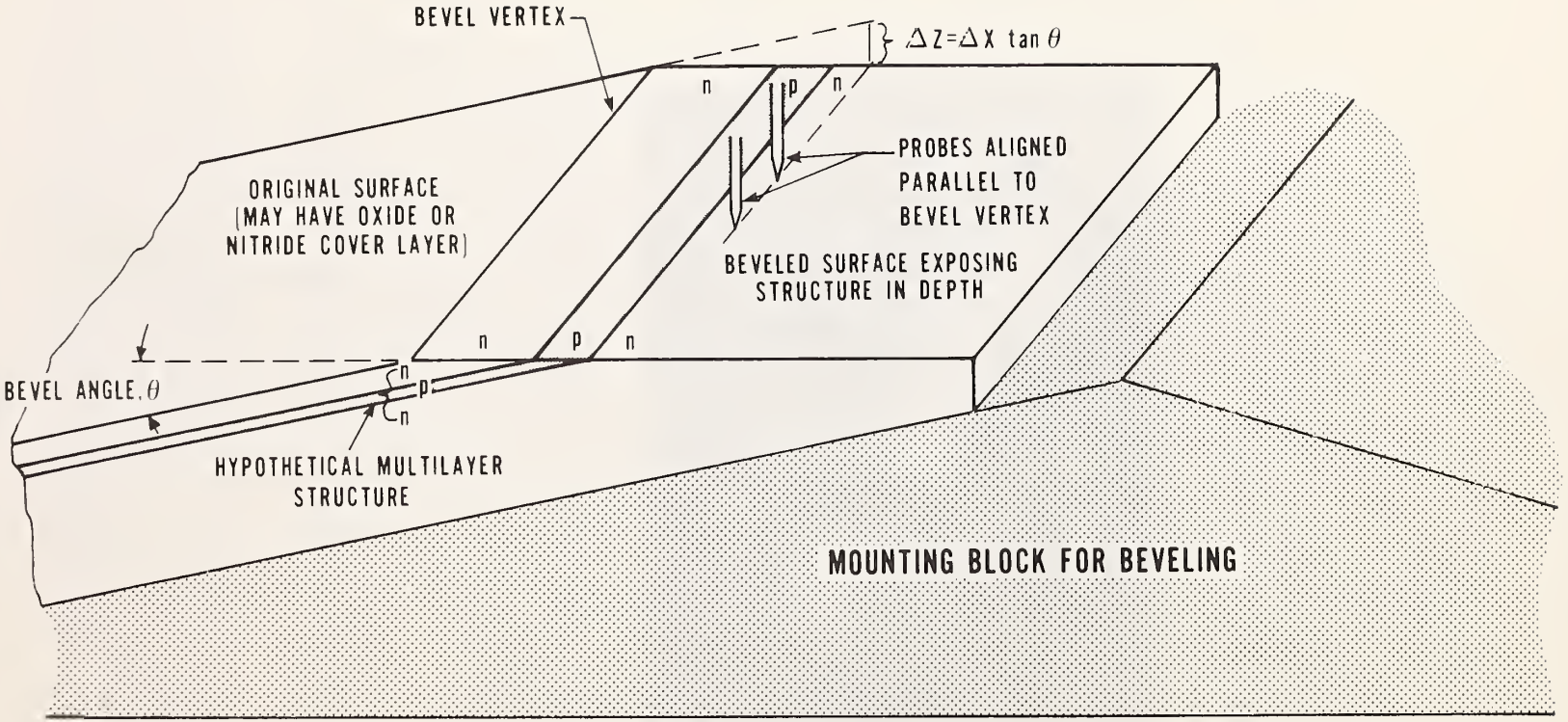

Figure 3-2. Schematic representation of a multilayer semiconductor structure which has been bevel-sectioned for depth profiling by spreading resistance probes.

In fact, despite the limitations and difficulties mentioned, spreading resistance measurements have been used for a number of years to obtain data for process control, for which there is little published in the literature [3-6], and for device design and modeling [3-7]. Such applications have a longer history for power control devices than for virtually any other type of semiconductor device. Figures 3-3 illustrates the application of this technique to screening of high resistivity n-type NTD and float-zoned silicon, respectively, for uniformity of lateral resistivity. Figure 3-4 illustrates the manner in which spreading resistance measurements are typically used for thyristor process control. In this figure, the numbered short line segments represent typical process control limits on position or absolute spreading resistance value of key profile features which are known to strongly influence thyristor operation. The position and size of these limits, or windows, are derived from spreading resistance profiles of properly operating thyristors which are sacrificed to acquire data for these process control limits. In such process-control-related measurements, reference to actual resistivity values as would be obtained through elaborate calibration and/or mathematical algorithms is not required. Direct spreading resistance data suffice for this purpose, provided that uncontrolled or extraneous variations, such as might be due to specimen preparation, are eliminated. Of course, for detailed analysis of profiles such as those resulting from new or modified process steps, raw spreading resistance data no longer suffice, and use of calibration data and of mathematical algorithms is required. Results obtained using very simple algorithms and less than optimal calibration procedures have generally been acceptable for the level of sophistication required for understanding the thyristor fabrication procedure. Discrepancies which occur between spreading resistance and other measurements are often remedied with empirical corrections based on experience or by acceptance of an unnecessarily large uncertainty in measurements. However, use of very simple algorithms and nonoptimized calibration slows the learning curve for state-of-the-art design changes such as may be required for thyristors for HVDC applications. Moreover, such procedures are inadequate for modeling, unambiguously, the mechanisms involved in thyristor operation.

3.3 Accomplishments This Year

Discussions were held in late 1977 with members of a number of thyristor research and production facilities regarding the strengths and weaknesses of spreading resistance measurements. The resulting evaluation [3-8] was the basis for the objectives in this subtask (see sec. 3-1).

3.3.1 Surface Preparation Procedures for Radial Profiling

Objective 3.1, identifying a silicon specimen preparation to improve the reproducibility of spreading resistance measurements on (111) n-type silicon, has been met. Four specimen preparations were chosen for study. All had the property of producing a nearly specular specimen surface which appears to be a necessary property for low point-to-point scatter of spreading resistance data. Two of the preparations were

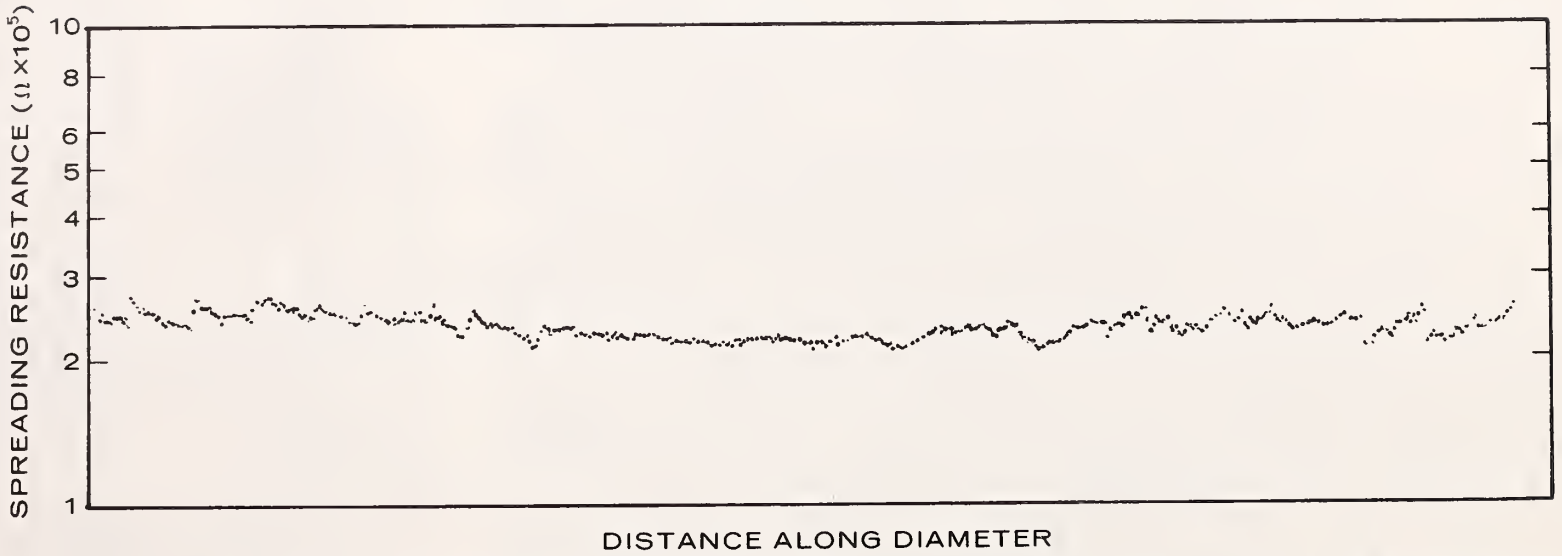

Figure 3-3a. Spreading resistance (resistivity) uniformity across the diameter of an approximately 60 Ω•cm NTD silicon slice.

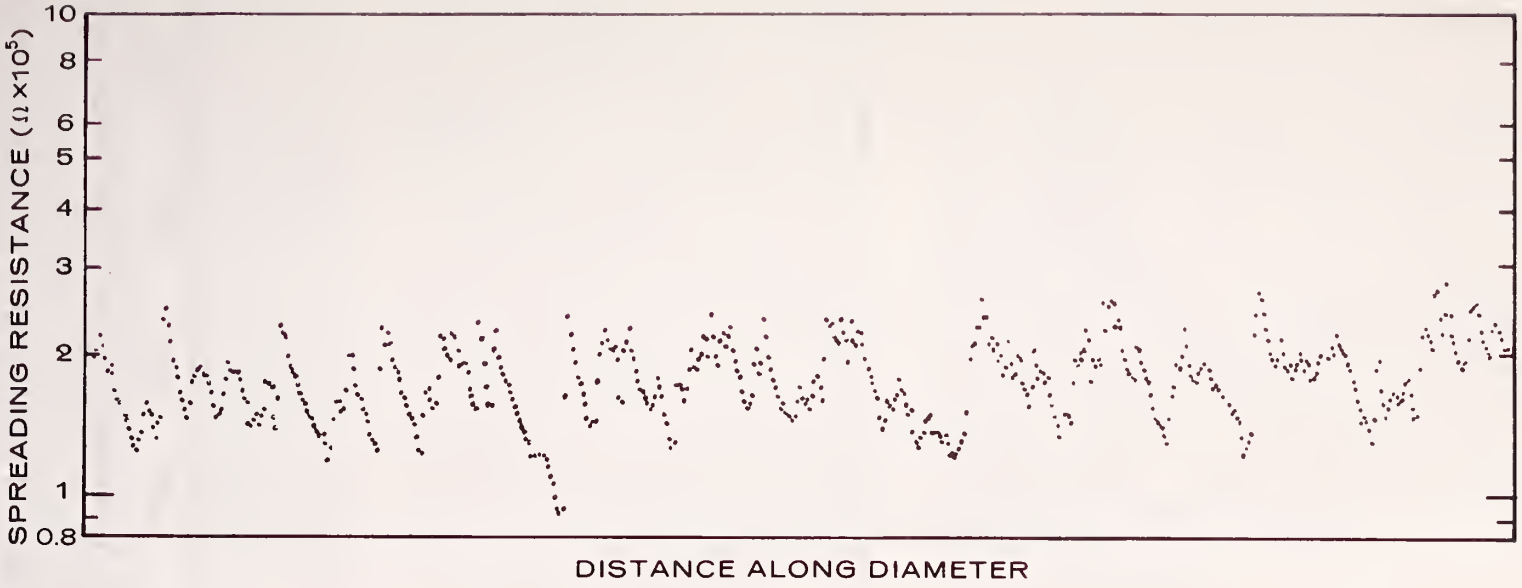

Figure 3-3b. Spreading resistance (resistivity) uniformity across the diameter of an approximately 60 Ω·cm standard float-zoned silicon slice.

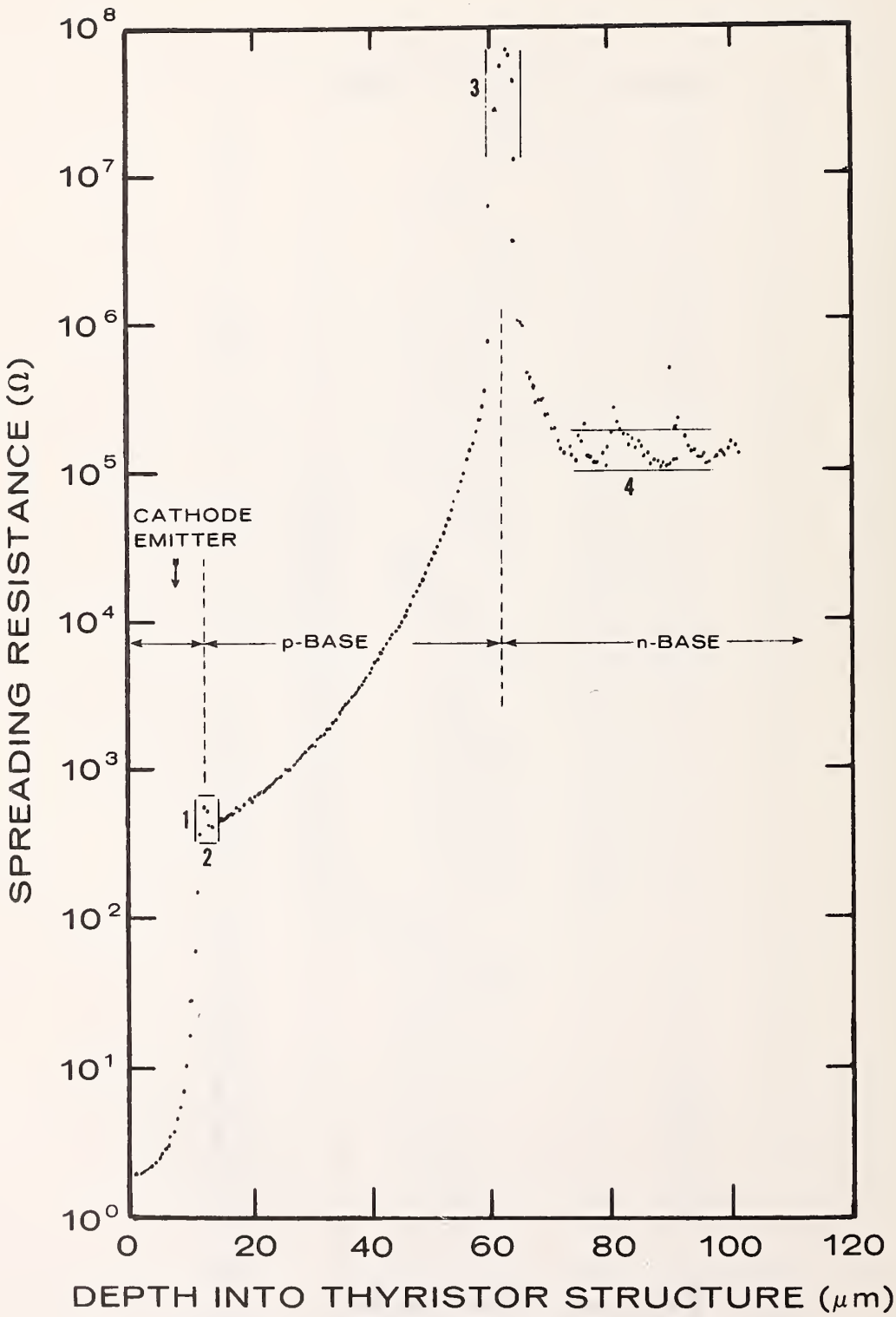

Figure 3-4. Spreading resistance profile of thyristor structure from cathode emitter side. Numbered vertical and horizontal bars show typical process control limits. (See text.)

based on chem-mechanical polishing with colloidal silica in an aqueous solution with a pH 10.5 to 11. One of these is obtained commercially as a premixed stabilized suspension; the other is obtained as silica powder which has to be mixed in aqueous suspension and an additive used to give the proper pH. The remaining preparations tested were based on mechanical polishing with diamond particles in a nonaqueous liquid. One of these used 0.5-μm polycrystalline diamond; the other used 3-μm polycrystalline diamond. Various auxiliary steps for cleaning, drying, and possibly stabilizing specimen surfaces were tested in conjunction with each of the four polish types. The polishing machine used was a laboratory scale oscillating tub polisher of the type most commonly used for preparing spreading resistance specimens. Tests were made on specimens from four crystals of NTD silicon and on specimens from three crystals of float-zoned silicon. The NTD silicon specimens were in the range from 30 to 400 Ω·cm and showed no resistivity fine structure striations. They were tested for reproducibility of average spreading resistance value and for point-to-point data scatter with repeated polishing by each process. The float-zoned silicon specimens were in the range from 30 to 150 Ω·cm and showed significant resistivity fine structure. They were tested for reproducibility of measurement of the extrema of such fine structure features following repeated polishing.

Complete details of the surface preparation procedures and the results of the measurements can be found in Appendix C. Results are illustrated here for 400 Ω·cm NTD silicon (fig. 3-5) and for 150 Ω·cm float-zoned silicon (fig. 3-6). Each figure consists of two parts: part (a) shows the results of spreading resistance measurements obtained after each step in a polishing cycle based on one of the silica polishes, and part (b) of each figure shows the results of spreading resistance measurements taken after each step of a polishing cycle based on 0.5-μm diamond. Comparison of part (a) with part (b) of each figure shows that clear superiority of measurement reproducibility is obtained by diamond polishing of the specimens. This superior reproducibility is also found at the other specimen resistivity levels as shown in the Appendix. Point-to-point repeatability on the NTD specimens (see tables C-2 through C-5 in Appendix C) was also found to be much better following diamond polishing.

Since spreading resistance is a transfer measurement requiring calibration on specimens of known resistivity, the improved measurement reproducibility following diamond polishing yields a twofold improvement in the measurement process. The first is improved precision of the calibration data; the second is improved precision in the interpretation of the specimen to be tested.

Both grades of diamond tested (0.5 and 3 μm) gave significant improvement of top surface measurement compared to results obtained following either type of silica polishing. The polishing pad used was a nonwoven cloth common in metallurgical polishing. A separate grade of this cloth was used for the two diamond polishes, based on the particle size of the diamond. Cleaning with acetone and dry methanol or similar water-free

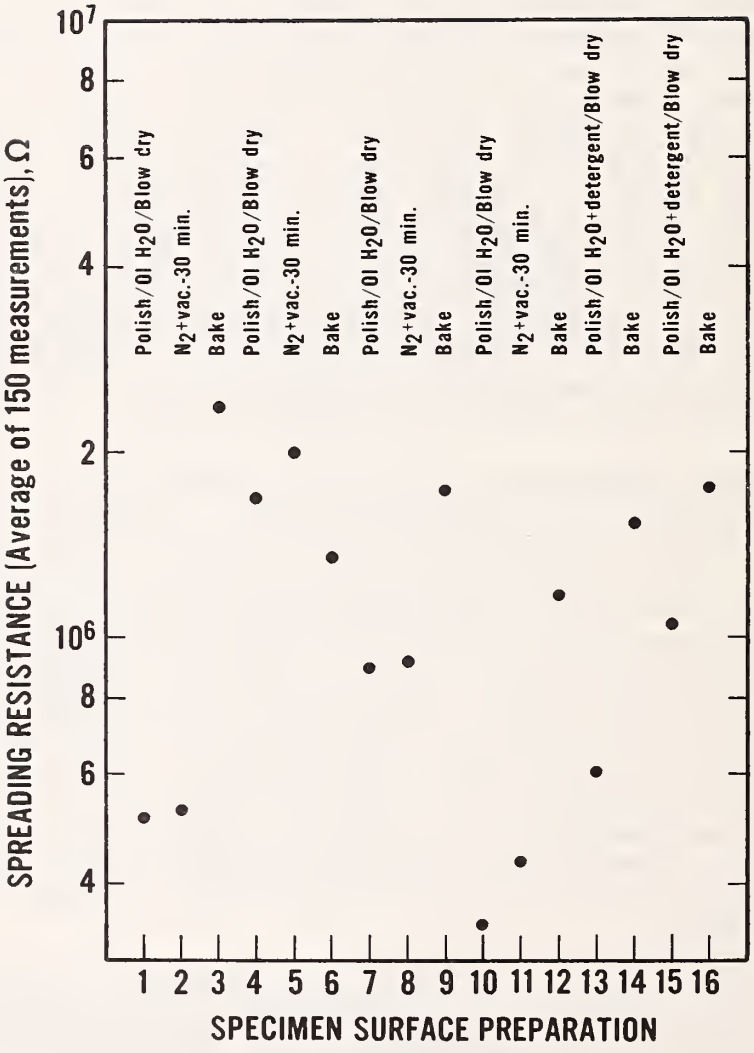

Figure 3-5a. Spreading resistance average *vs*. surface preparation: colloidal silica series — 400 Ω·cm NTD silicon specimen.

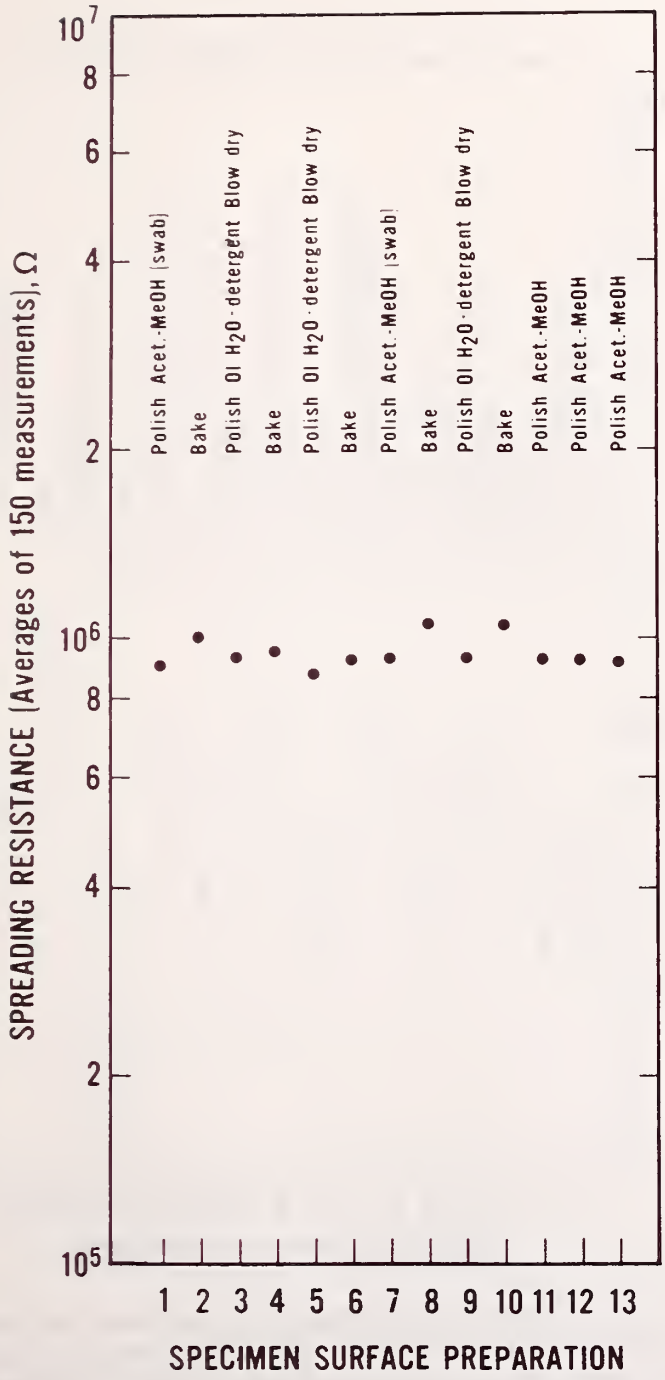

Figure 3-5b. Spreading resistance average *vs.* surface preparation: 0.5-μm diamond polish series — 400 Ω•cm NTD silicon specimen.

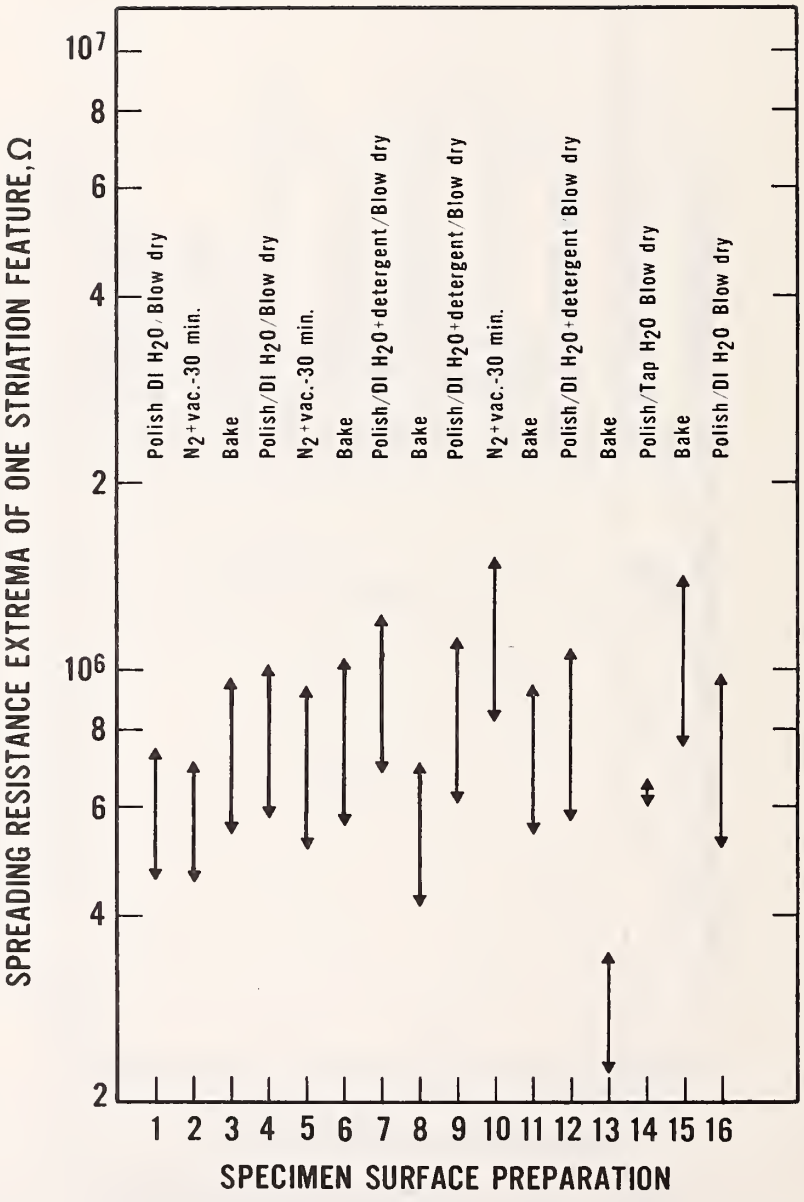

Figure 3-6a. Spreading resistance maximum and minimum *vs.* surface preparation for one resistivity striation feature: colloidal silica series — 150 Ω·cm float-zoned silicon specimen.

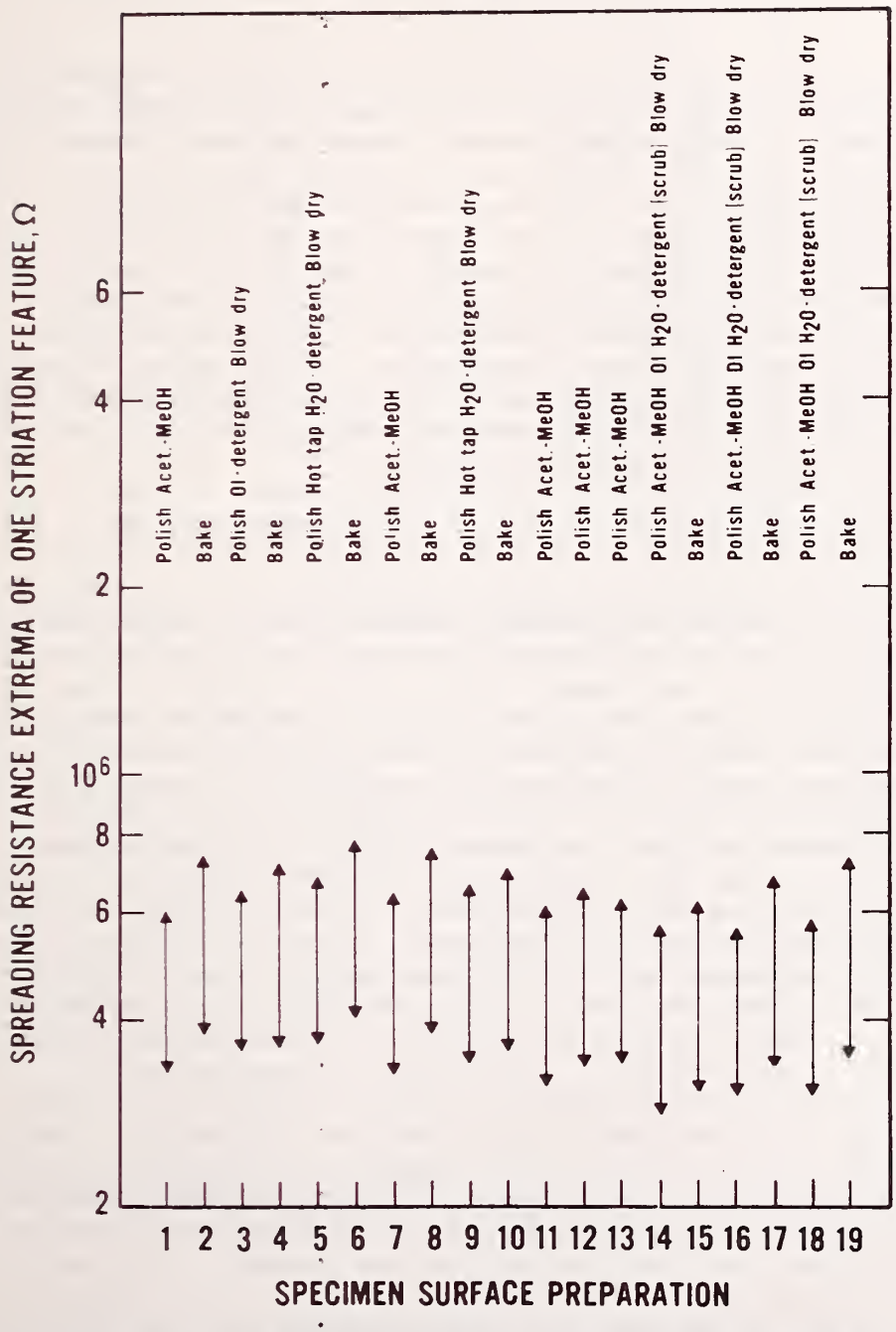

Figure 3-6b. Spreading resistance maximum and minimum *vs.* surface preparation for one resistivity striation feature: 0.5-μm diamond polish series — 150 Ω•cm float-zoned silicon specimen.

solvent is recommended, although specimen cleaning with water and detergent appears to be satisfactory. Finally, the post-polishing baking step, generally found advisable after aqueous polishing [3-2,3-9], is not necessary after diamond polishing.

It is desirable to extend diamond polishing to specimen beveling for depth profiling, at least where the specimen contains high resistivity *n*-type layers. For this application, a work surface is needed which is much harder (less compressible) than the cloth used for top surface polishing. When using such a hard surface, the scratch damage to the specimen increases compared to the damage obtained with the nonwoven cloths used for top surface polishing. Since point-to-point measurement scatter is controlled in part by the uniformity of the surface, it is desirable to minimize this scratch damage. Although both grades of diamond tested gave satisfactory results for top surface preparation of specimens, the 0.5-μm diamond results in a smoother specimen surface. This advantage makes 0.5-μm diamond preferable for testing the extension of diamond polishing to specimen beveling.

3.3.2 Surface Preparation Procedures for Depth Profiling

Objective 3.2, extending the diamond polishing process developed under objective 3.1 to bevel sectioning of thyristors for depth profiling, was also achieved. The feasibility of specimen beveling using diamond compound was tested in two stages, first on bulk specimens, then on thyristor structures. As shown in section 3.3.1, diamond polishing was found to give reproducibility of spreading resistance measurements superior to that obtainable with colloidal silica polishing for high resistivity *n*-type specimens. However, it has been general experience that silica polishing followed by specimen baking (150°C for 15 min) gives good measurement control for low resistivity (111) *n*-type and for the entire resistivity spectrum of *p*-type silicon. To be acceptable for general use in spreading resistance measurements on silicon, diamond polishing should yield measurements for this extended spectrum of specimens with a quality similar to that already obtainable with silica polishing. Tests were made on sets of (111) *n*- and *p*-type silicon specimens spanning the resistivity range from 0.001 to 400 Ω•cm and mounted for use as spreading resistance calibration blocks. Comparisons were made of the quality of spreading resistance measurements obtained following polishing of these specimen blocks with 0.5-μm diamond and with silica. The results, detailed in Appendix D, show that acceptable measurement control can be obtained for both conductivity types over the entire resistivity range when the surfaces are polished with 0.5-μm diamond. The results obtained on diamond-polished specimens are, in fact, very similar to those obtained on silica-polished and baked specimens but have the advantage of being more reproducible and more linear with specimen resistivity for high resistivity *n*-type specimens.

Since polishing with 0.5-μm diamond yields high quality spreading resistance data throughout the range of resistivities encountered in device structure, it should be adaptable to bevel sectioning for depth profil-

ing of thyristors and other devices. However, it was found that to validly transfer the calibration data to bevel-sectioned specimens it was necessary to reduce to 0.1 μm the size of the diamond particles used for beveling. This change is due to the fact that the calibration specimens were designed to be prepared by top surface polishing against cloth, whereas the beveling procedure must be done against a much harder surface (frosted glass was used) to maintain control of bevel geometry. As a result, it was necessary to use a smaller grit diamond in conjunction with the glass surface polishing to get an equivalent specimen surface condition and an equivalent spreading resistance response.

Depth profile measurements were made on three commercial thyristors to compare the results obtainable by diamond beveling with those obtainable by the more traditional silica polishing. Separate specimens were used for each polishing procedure. Figure 3-7 shows spreading resistance depth profile data on a specimen of one of the thyristors which was beveled with 0.1-μm diamond; part (a) shows data for the cathode emitter, p-base and part of the n-base at moderate depth resolution; and part (b) shows data at higher resolution for just the cathode emitter and p-base. Figure 3-8 shows corresponding depth profile data taken on an adjacent specimen of the thyristor which had been bevel-sectioned with silica polish and baked prior to measurement in the manner recommended for control of p-type layers [3-9]. Slight apparent differences in the depth scales of these figures are due to slightly different bevel angles.

Based on the good agreement already found between measurements on diamond-polished surfaces and silica-polished and baked surfaces of low resistivity n-type and all p-type calibration specimens, good agreement is also expected for the cathode emitter and for the p-base layer data of the thyristor sections similarly prepared. Such agreement is seen, in fact, when comparing corresponding figures 3-7b and 3-8b. Further, based on the improved reproducibility of spreading resistance measurement on high resistivity n-type layers which have been diamond polished, it is expected that the n-base resistivity values from the diamond-beveled thyristors are in better agreement with independently measured values than are those from the silica-beveled thyristors.

3.3.3 Summary of Benefits of Specimen Preparation by Diamond Polishing

Significant improvements in the quality of spreading resistance measurements have been shown to result from diamond polishing, both for surface measurements of starting material and for depth measurements of devices

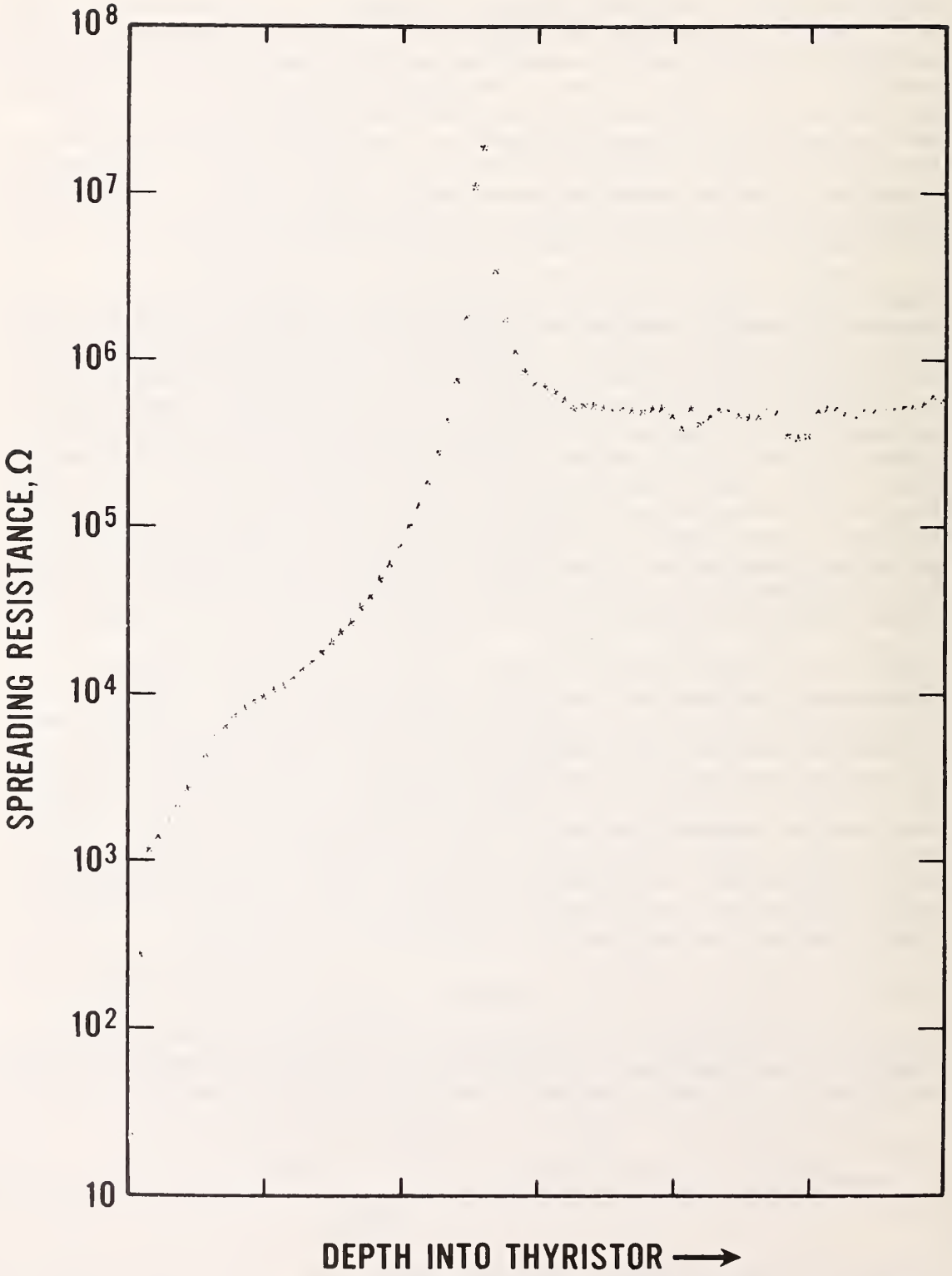

Figure 3-7a. Raw data for cathode emitter, *p*-base and part of *n*-base thyristor I, 0.1-μm diamond-beveled specimen, 25-μm step size.

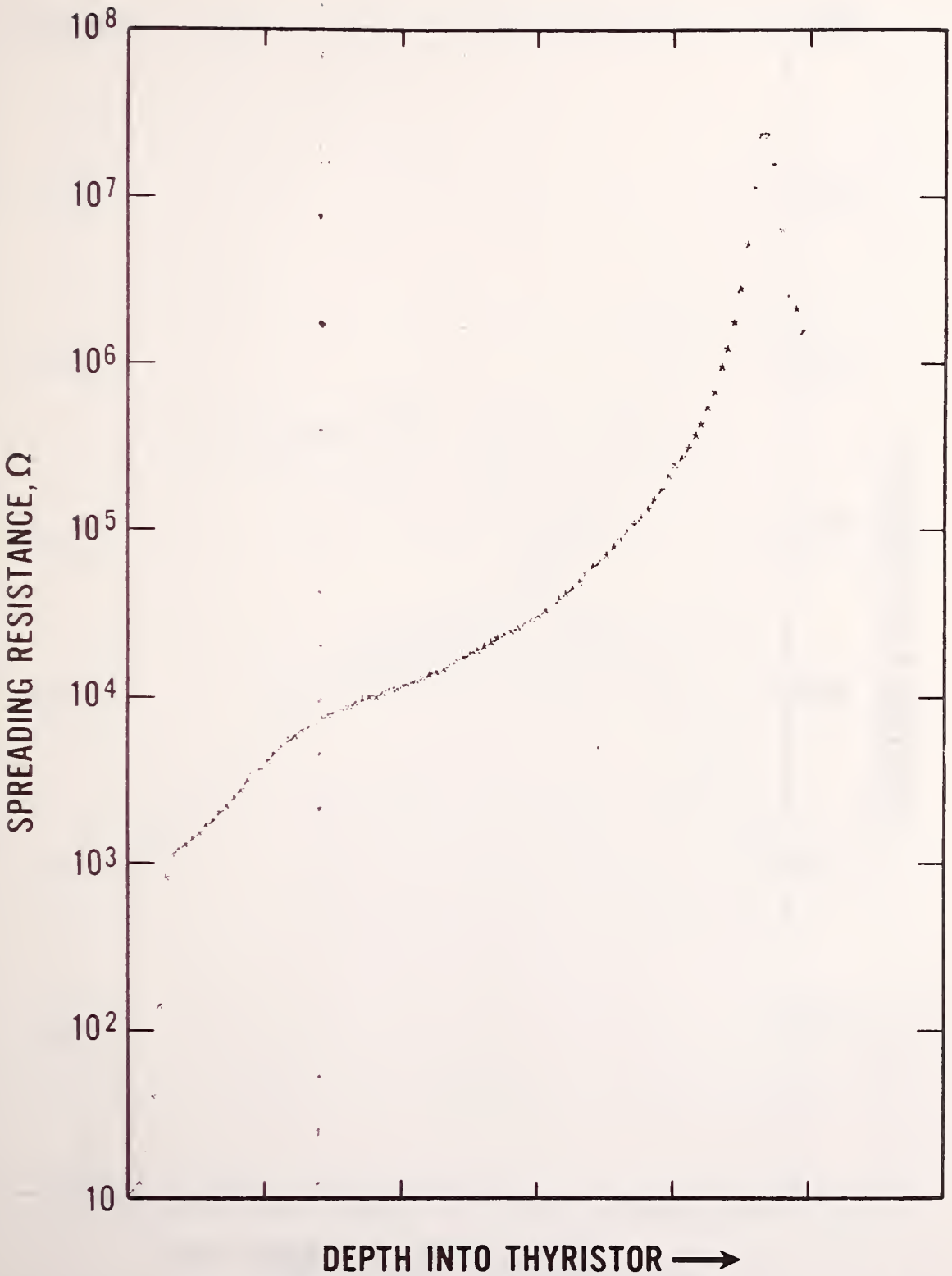

Figure 3-7b. Raw data for cathode emitter, *p*-base thyristor I, 0.1-μm diamond-beveled specimen, 10-μm step size.

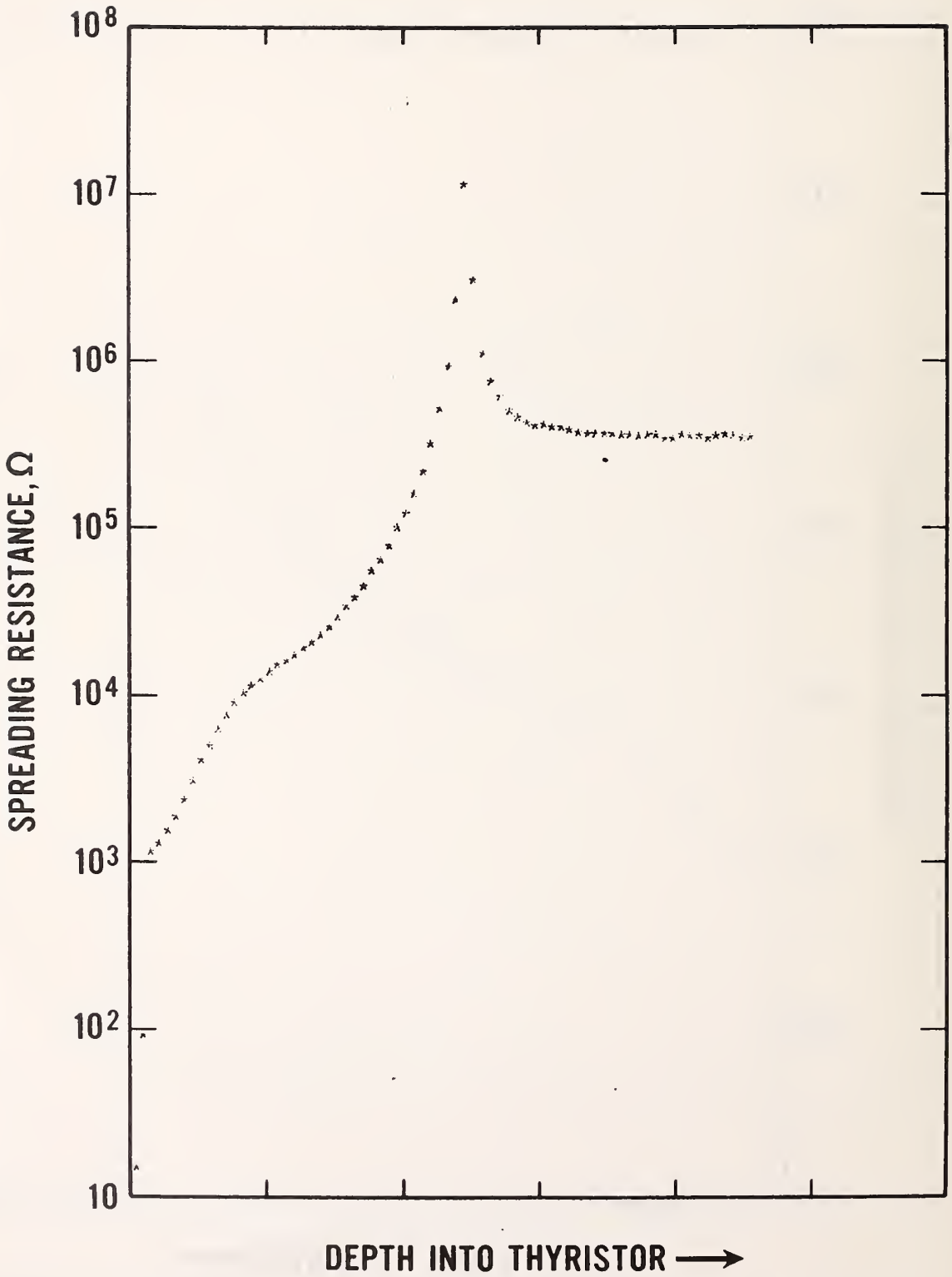

Figure 3-8a. Raw data for cathode emitter, *p*-base and part of *n*-base thyristor I, colloidal silica-beveled and baked specimen, 25-μm step size.

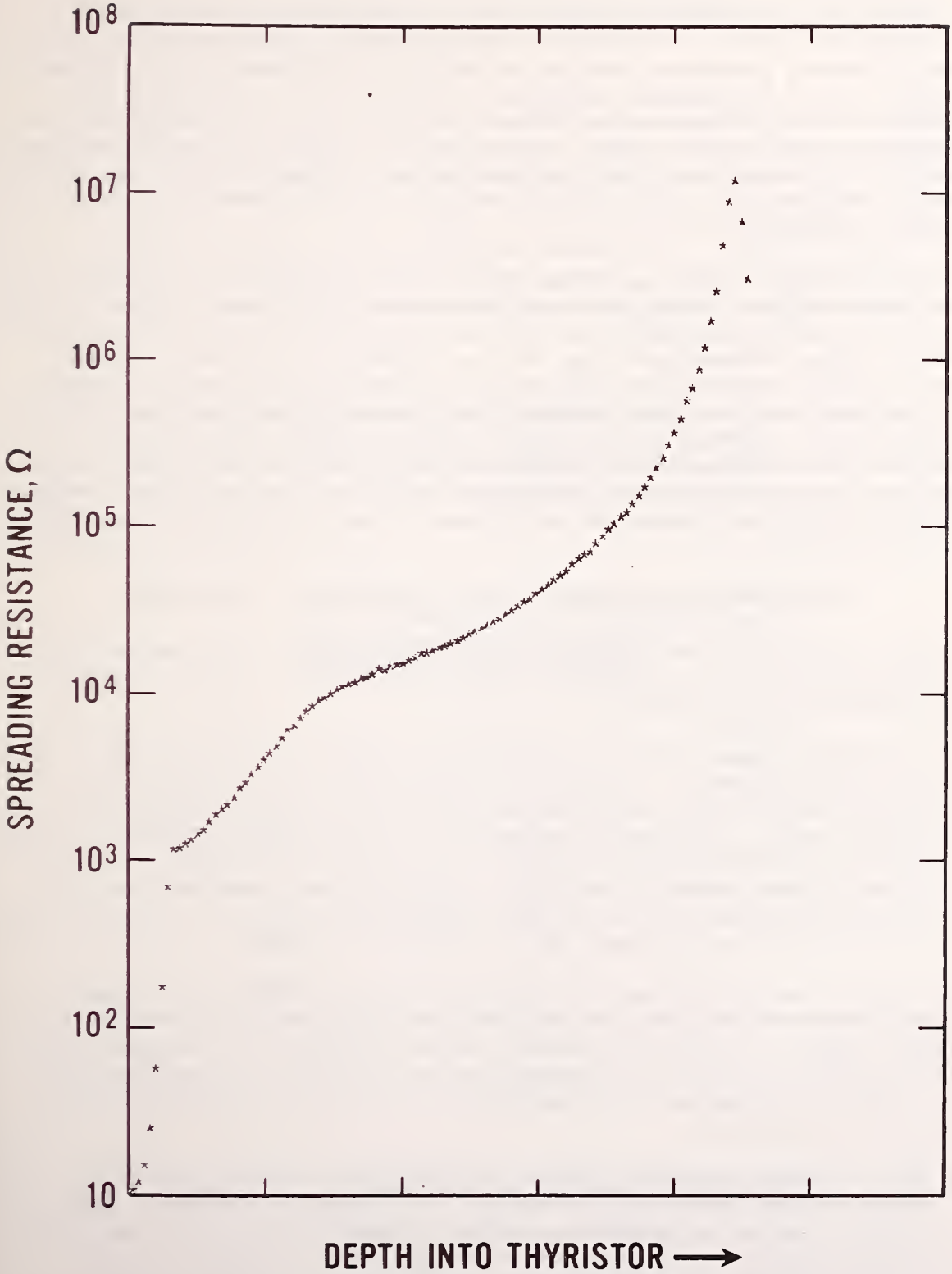

Figure 3-8b. Raw data for cathode emitter, *p*-base thyristor I, colloidal silica-beveled and baked specimen, 10-μm step size.

(thyristors) where high resistivity n-type silicon is involved.*

The polishing processes found to be preferable were designed to allow a single set of calibration specimens to suffice for both surface and depth profiling measurements. These processes are: polishing with nonaqueous 0.5-μm diamond slurry against nonwoven cloth for large area top surface polishing (both calibration and test specimens) and bevel polishing with nonaqueous 0.1-μm diamond paste against frosted glass for depth profiling.

It is possible to gain additional advantages by optimizing separately the preparation of large area and bevel section specimens at the cost of requiring separate calibration sets for each type of measurement. The use of larger diamond grit, up to 3 μm, speeds the polishing of large area slices. Calibration specimens for this procedure must, of course, be polished with the same (larger) size diamond. For depth profiling applications, diamond beveling against ground glass could be used to prepare both calibration and test specimens. The use of 0.1-μm diamond for both types of specimens would provide better surface quality, while the use of 0.5-μm diamond for both types of specimens would allow higher polishing rates.

3.3.4 Dopant Species Dependence on Calibration for p-Type Dopants

Objective 3.3, to test the dopant species dependence of spreading resistance measurements for p-type silicon, was reached. Complete results are given in this section.

It is fairly common practice to use some combination of boron, gallium, and aluminum dopants to obtain the thick, graded p-type layers found in thyristor structures. All three have similar acceptor levels in the band gap, and it is generally assumed that they behave similarly insofar as spreading resistance measurements are concerned; calibration data obtained on more readily available boron-doped bulk specimens are used for interpretation of gallium- and aluminum-doped layers. However, formal equivalence had not previously been demonstrated.

A limited test of this equivalence was conducted. Five boron-doped, four aluminum-doped, and two gallium-doped specimens were used in this test. Table 3-1 lists the nominal resistivities of the specimens used. To minimize any possible discrepancies due to effects of specimen size on surface preparation, all specimens were slices of comparable size;

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* Use of diamond polishing against frosted glass also results in improved control over bevel geometry. This geometry control allows beveling at angles as shallow as several minutes of arc. Although these shallow angles are not necessary for profiling of thyristor structures, they must be used for depth profiling of shallow integrated circuit structures whether or not high resistivity n-type layers are involved.

the composite calibration block of boron-doped specimens was not used. The resistivity range of the five boron slices was slightly larger than the combined gallium-aluminum range.

Four-probe resistivity values were measured on each slice, and spreading resistance radial profiles were taken to measure resistivity nonuniformity. Each of the species was polished at least four times, baked, and measured. The measurements consisted of 25 spreading resistance values at increments of 50 μm. The order of specimen measurements was continually randomized. Spreading resistance measurements were taken near, but generally not at, the center of the slices, so that an averaging of the variations seen in the spreading resistance radial profiles could be obtained.

A summary of the data is found in figure 3-9. The scatter in the symbols for any one specimen generally correlates with the amount of resistivity variation originally seen in the radial profiles for that slice. Based on this set of measurements, it is concluded that no significant difference can be found between boron-doped silicon and either aluminum- or gallium-doped silicon insofar as spreading resistance calibration is concerned.

Table 3-1. Resistivity Values of Specimens Used to Test Comparability of Spreading Resistance Measurements on Boron-, Aluminum-, and Gallium-Doped Silicon.

Boron	Aluminum	Gallium
0.121 Ω•cm	0.692 Ω•cm	1.54 Ω•cm
1.072 Ω•cm	1.14 Ω•cm	2.31 Ω•cm
4.98 Ω•cm	4.62 Ω•cm	
10.5 Ω•cm	9.30 Ω•cm	
17.6 Ω•cm		

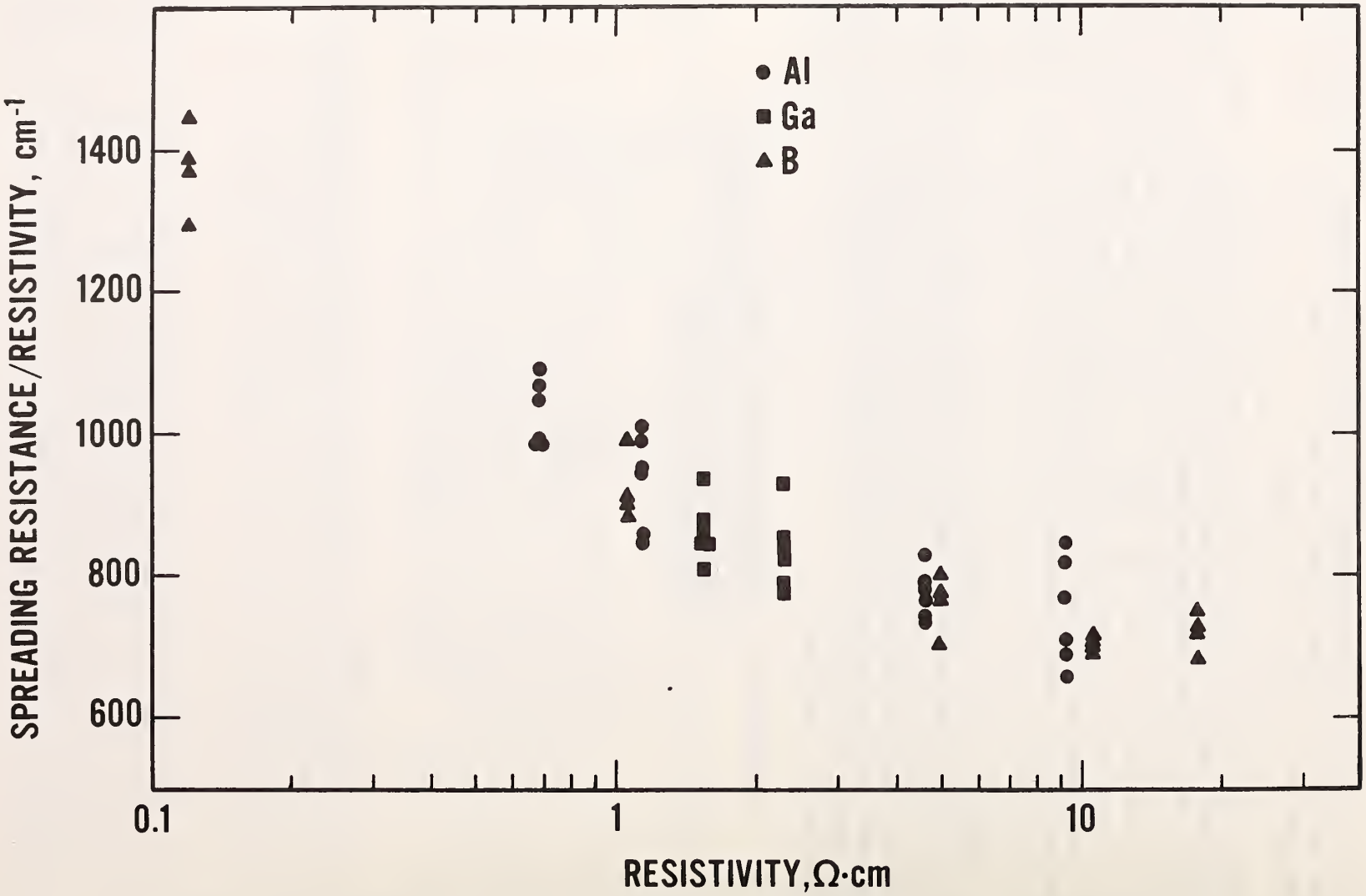

Figure 3-9. Spreading resistance response for three different p-type dopants.

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Appendix A

Fabrication Procedures

This appendix provides additional details on the fabrication procedures which were developed under this study. This includes mesa etching procedures, mesa passivation, and contact metallization.

A-1 Mesa Etching Procedures

The first major step in the processing of diffused wafers for the mesa diodes is the mesa etching or junction isolation procedure (see fig. 2-1). Of the four proposed techniques [A-1, p. 32], three (ultrasonic machining, plasma etching, and chemical etching) were implemented and evaluated. The plasma etching technique, utilizing a commercial machine, was by far the most reproducible and straightforward method. This technique was adopted for the fabrication procedure and is discussed in detail. Also provided are some previously unreported details on the ultrasonic machining method.

Plasma Etching of Mesas — Early attempts at plasma etching of the mesa structure resulted in diodes with satisfactory electrical characteristics [A-2, pp. 54-55]; however, the etch rate was found to be too low for practical fabrication of the deep mesa required on power device wafers. Typically, mesas with depths of a few micrometers required about 20 min to etch. Although the etch rate was low, the electrical characteristics of the resulting devices and the relative stability of the processing encouraged further investigations to improve the method.

The plasma etching procedure of a mesa diode structure consists of: 1) wafer cleanup, 2) application of the mesa masking material, 3) definition of the mesas, and 4) plasma etching. A variety of mesa masking materials was tested. These included photoresist, thermal oxide, chemical-vapor-deposited (CVD) oxide, metal films, and various combinations thereof. The simplest and most straightforward technique was to use an evaporated aluminum film as the masking agent. The mesa definition was accomplished by photolithography of the aluminum film.

The basic physical and chemical reactions governing plasma etching are not well understood. However, by empirical adjustment of the various parameters available, a set of conditions was found which results in a satisfactory etch rate. The system* in use is a barrel type reactor with an rf-excited plasma. The etching reaction occurs at a pressure of 50 Torr using a mixture of 4-percent oxygen in Freon-14; the rf power was set at 200 W. Under these conditions, the etch rate was essentially constant and time was used to adjust the etch depth.

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*International Plasma Corporation, Hayward, California, Model 2000.

Figure A-1 shows a plot of the etch depth against the etch time. The open circles are data from wafers individually etched, but at different times, with the machine parameters reset each time. The solid circles represent wafers etched individually for the given time for a controlled experiment (all parameters carefully monitored). The squares represent the sum of the etched depths when multiple wafers were etched simultaneously. As indicated by the open circles and some of the squares, there are deviations in the etching depth due to variations in parameter control or loading effects on the plasma. However, the general indication is that the etch depth is linear with time and appears to be inversely proportional to the area of silicon being processed; this is probably due to the finite number of chemically active species which are available in a given amount of time to react with the silicon. By using this technique, deep mesa structures of 75 μm could be fabricated routinely with good depth control in times of about 100 min.*

Figure A-2 shows a photomicrograph of a typical plasma-etched wafer. The masking agent was an aluminum film patterned with mask level one of test pattern NBS-13 [A-1, p. 35]. The light areas are the p^+-regions which were protected by the mask, and the dark regions show n^--areas where the plasma process has removed the p^+-silicon. The cell size is 5.08 by 5.08 mm and the etched depth in this case is about 53 μm. The arrow points to one of the small circular devices, and a close inspection reveals some interesting features of the plasma etching reaction. Figure A-3 is a photomicrograph of this mesa. The lithographically defined mesa diameter of this structure is 254 μm. Two things are evident from this figure: 1) there is significant lateral etching by the plasma and 2) there is an obvious preferential crystallographic direction for the plasma reaction. The diameter of this device is 140 μm (across the "flats") to 150 μm (across the corners); it is evident that the plasma reaction occurs at approximately the same rate horizontally as it does vertically. The slight preferential etching in crystallographic directions distinctly reveals the sixfold symmetry of this <111> surface.

The lateral etching or the mask undercut during the plasma etching procedure is similar to that experienced during chemical etching. However, the plasma procedure was highly controllable and resulted in uniform removal of silicon. In most cases, there were no failures as a result of mask liftoff. Nevertheless, the lateral etching caused many of the smaller devices of test pattern NBS-13 to be ill-defined after deep mesa etching procedures.

Ultrasonic Machining of Mesas — Ultrasonic machining is accomplished by vibrating a specially designed tool head against the silicon wafer in the presence of an abrasive slurry. The tool head is designed to remove

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*Although this etch rate is not unreasonable, it is likely that a plasma machine specifically configured for silicon etching could have a much higher etch rate with good control.

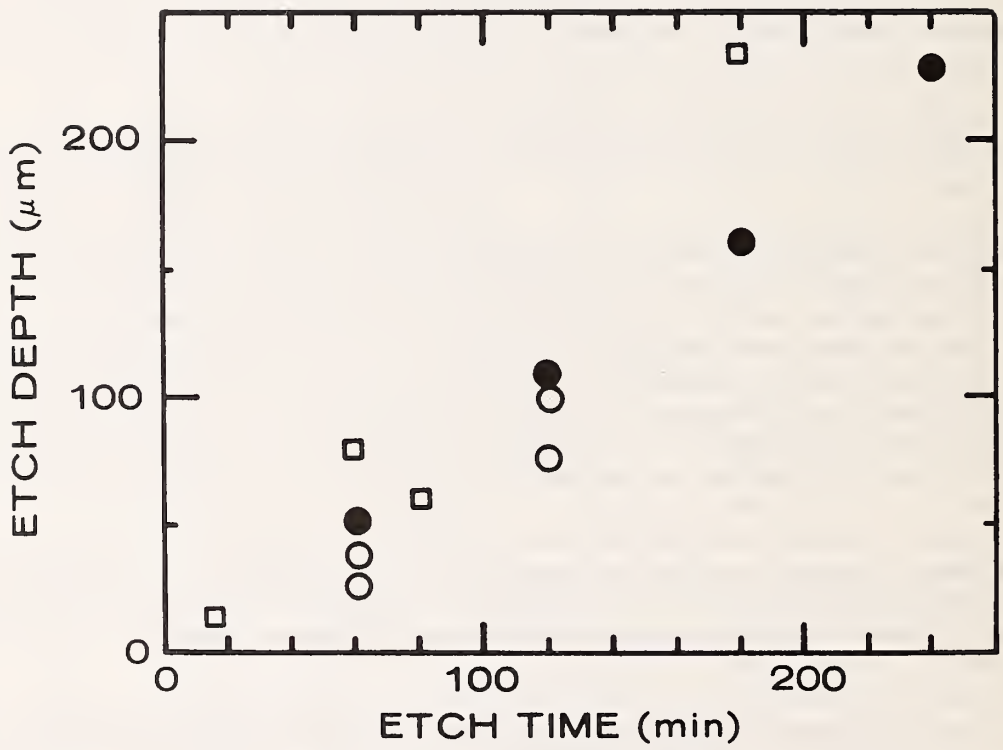

Figure A-1. Plot showing etch depth of silicon against etch time in the plasma etching machine.

Figure A-2. Photomicrograph of plasma-etched mesas. The arrow indicates a particular device which is enlarged in figure A-3. See text for discussion of details.

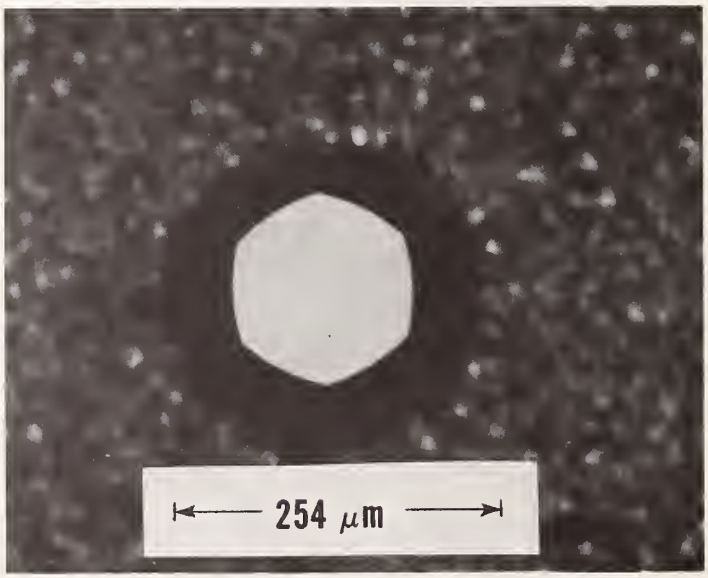

Figure A-3. Photomicrograph of a plasma-etched mesa whose mask dimension was 254 μm in diameter.

unwanted p^+-regions surrounding each of the mesa diodes being fabricated. Figure A-4 is a photograph of a tool machined for this purpose. This tool was designed to form mesas about 1.5 mm in diameter, spaced at 5.08 mm in each direction. These dimensions are compatible with the contact window and metallization mask levels for existing test patterns. In order to minimize ultrasonic machining of unnecessary areas, p^+-regions between mesas are left undisturbed by slotting the tool head. The left side of figure A-5 shows a photograph of the wafer after the ultrasonic machining operation; the wafer after opening the contact windows and defining the metallization is shown on the right. Only the ultrasonically machined mesas near the center are usable devices. The other patterned devices near the perimeter of the wafer are simply metallization patterns on p^+-regions resulting from the masking operation.

Mesa diodes as deep as 100 μm were successfully fabricated using this ultrasonic machining technique. Because the machining is mechanical in nature, the contour of the mesa wall (i.e., vertical or sloping) can be controlled by appropriate design of the tool. In addition, the depth of the cut can be monitored during the progress. A major disadvantage of the technique is the necessity to fabricate the special tool head; the tool must be machined with high precision in order to allow compatibility with subsequent photomasking steps. Tool wear also necessitated regular resurfacing and recontouring of the cutting surface.

A-2 Mesa Passivation

In the earlier processing of mesa diodes, the passivation step consisted of a hydrogen-peroxide-based cleanup and growth of a dry thermal oxide. The dry thermal oxide, whose properties are well understood, was initially used to minimize the influence of the passivation layer on the other process procedures being evaluated. However, it is not acceptable for this mesa fabrication process since it requires a 1000°C oxidation temperature which could possibly alter the properties of the wafer being evaluated. Hence, efforts were directed toward identification of a suitable lower temperature passivation procedure.

There is a variety of passivation-protection techniques used by the power thyristor industry. In particular, the use of glasses, varnishes, room temperature vulcanizable rubbers, and other proprietary recipes are common. These materials are optimized for the operating temperature range of the device and, in general, would not necessarily be suitable for the mesa structures being fabricated under this study. Specifically, the mesa structures for deep level studies should be capable of being physically cycled between liquid nitrogen temperature (77 K) to over 350 K with heating rates as high as 7 to 10 K/s.

Chemical-vapor-deposited silicon dioxide (CVD-SiO_2) proved to be satisfactory as a passivation-protection layer. Although CVD-SiO_2 is generally less dense than thermal SiO_2, appropriate care and treatment allows it to be photolithographically patterned much like thermal sili-

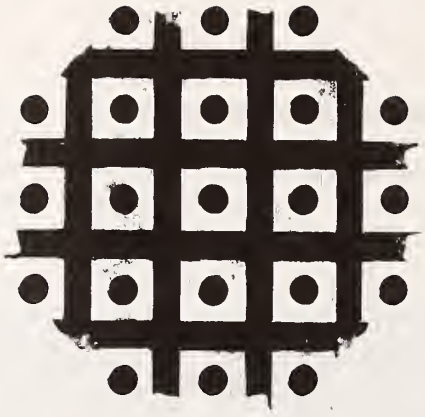

Figure A-4. A photograph of the face of a tool head for forming mesa diodes by ultrasonic machining. The overall size of the face is approximately 25 by 25 mm.

Figure A-5. The left wafer (a) shows the result of the ultrasonic machining procedure on the *pnp*-diffused wafer (51-mm diameter). The right wafer (b) shows the results after passivation and contact metallization.

con dioxide. CVD-SiO_2 has also been successfully used as the insulating layer in the fabrication of low temperature metal-insulator-semiconductor (MIS) structures which could be used for deep level characterization of starting material [A-2, pp. 22-27; A-3]. The CVD-SiO_2 is applied* at 400°C by the pyrolytic decomposition of silane (SiH_4); this temperature is considerably lower than that required to grow thermal silicon dioxide and, as a consequence, eliminates or minimizes alteration of the material under study due to high temperature effects. In general, the transition from the use of thermal silicon dioxide to CVD-SiO_2 was not detrimental to the quality of the mesa diode properties.

A-3 Contact Formation

Contact metallizations to lightly doped n-regions can be accomplished by phosphorus diffusion and aluminum metallization. Although the aluminum metallization is not objectionable in this case, the high temperature (1000°C) diffusion is. A lower temperature alternative would be highly desirable, and efforts here have led to a viable alternative. Antimony-doped gold (Au-0.6% Sb) is routinely used for contact to n-type silicon in the 5 to 10 Ω·cm range. It was also found to be usable for the n^--region of thyristor material which usually ranges from 20 to 150 Ω·cm. The metal is applied by thermal evaporation with the wafer at or near room temperature. However, it is necessary to assure that the contact openings are as free as possible from oxide. The presence of such an oxide generally inhibits the alloying process into the silicon. The present processing steps allow for a 400°C, 20-min microalloy in dry nitrogen prior to the photolithographic definition of the n^--contact regions.

Contact to the diffused p^+-regions was made with aluminum. Usually the surface concentration of the diffused regions is high enough that a microalloy is not necessary. Hence, after photolithographically etching the p^+-contact openings on the tops of the mesas, aluminum is evaporated and then photolithographically defined. In addition to providing p^+-contact, aluminum is also photolithographically defined over the previously applied gold-antimony n^--contact. This aluminum layer over the gold-antimony layer improves the durability of the contacts during probing for measurement. The presence of aluminum over the gold layer provides the necessary ingredients for the possible formation of gold-aluminum intermetallic compounds (i.e., purple plague) [A-4]. Hence, it is necessary to avoid overheating of the wafer during the course of any measurements or other treatments that follow this step.

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*Unicorp, Inc., Sunnyvale, California, Model Rotox 60.

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Existence of an isotope shift for the sulfur deep level in silicon[a)]

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(Received 13 February 1978; accepted for publication 28 March 1978)

The deep energy level of the isotope ^{34}S in the upper half of the energy gap of silicon is examined by isothermal transient capacitance measurements on ion-implantation-predeposited diode structures. The resulting energy level at $E_c - 0.512$ eV is found to be 0.014 eV closer to the conduction band edge than the corresponding deep level for the isotope ^{32}S in similarly prepared samples. The existence of an isotope shift for the deep sulfur level is interpreted as implying vibronic coupling between the electronic states of the sulfur center and the silicon lattice.

PACS numbers: 71.55.Fr, 63.20.Mt, 61.70.Tm

Successful calculations of the energy levels of sulfur in silicon have been performed in both the multivalley-effective-mass approximation[1] and in the effective-mass approximation in the pseudopotential formalism.[2] These treatments neglect the interaction of the electronic wave functions for the deep sulfur impurities with the lattice phonons. Other theories of deep levels in semiconductors have predicted strong coupling between phonons and the impurity wave functions; either as due to the dynamic Jahn-Teller effect[3] or to lattice relaxation.[4] Purely electronic transitions between levels characterized by this coupling of *vibrational* and *electronic* wave functions (i.e., vibronic levels) can exhibit an isotope shift that can be related to the difference in the zero-point energies of the vibrations between the isotopes.[5] In a previous paper,[6] we have characterized the energy levels of ion-implantation-predeposited ^{32}S in silicon by thermally stimulated current and capacitance measurements. These results were in good agreement with previous studies of the energy levels of sulfur diffused into silicon.[7] The natural abundance of ^{32}S is 95%.[8] The present paper reports the deep energy level of ^{34}S in silicon and demonstrates the existence of an isotope shift in the sulfur deep level.

As in our previous study of the energy levels of ^{32}S in silicon, the structures used for this study were Devices No. 9 and 19 of test pattern NBS-2,[9] p^+-n junctions fabricated on 5–10 Ω cm ⟨111⟩ n-type silicon wafers. Boron predeposition and diffusion through 1.53- and 2.06-mm-diam openings in 500 nm of fixed oxide formed the 450-nm-deep p^+ region. During drive in, approximately 30 nm of oxide were regrown over the p^+ region to seal the wafer. The isotope ^{34}S was implanted at 140 keV to a dose of 1×10^{13} cm^{-2} by rastering the beam over the wafer surface. Comparison of the singly ionized currents at mass 32 and mass 34 indicated that the mass 34 beam was at least 95% ^{34}S. The implant was followed by a 10-min 1000 °C anneal in dry nitrogen, and then approximately 150 nm of oxide were chemically deposited at 400 °C to increase the thickness of the oxide over the diffusions. This was followed by a 15-min 1000 °C heat treatment in dry nitrogen to densify the deposited oxide and further diffuse the sulfur. Contact cut, top metallization (aluminum), back metallization (gold plus 0.6% antimony), top metal definition, and a 10-min 500 °C microalloy in dry nitrogen completed the fabrication of the structure. A field plate around the diode was provided to control any leakage at the junction periphery. Unlike other procedures,[10,11] the present procedure eliminates implantation damage from the p-n junction region to prevent damage levels from interfering with the deep-level signatures of the implanted species. In this procedure, the near-surface p-n-junction boundaries are located under the field oxide due to lateral diffusion during junction formation, and thus can be shielded from implantation damage by the proper choice of field oxide thickness. Similarly, the p-n-junction boundary located under the opening in the field oxide can be protected from implantation damage by the proper choice of beam energy. In the present experiment, the sulfur distribution has a projected range 120 nm below the silicon surface with a projected standard of approximately 57 nm [12]; these values are far smaller than the 450-nm depth of the diffused p region. Thus, due to the design of the present experiment, the deep-level signatures observed are due only to implanted impurities that have diffused to the junction boundaries.

The energy levels for the sulfur defects were measured by the isothermal transient capacitance technique.[13] Basically, this technique measured the decay of the diode-depletion capacitance transient at a carefully regulated (±0.02 K) temperature, as the emission from charged defects allows a differential collapse of the depletion region. The time constant of the capacitance decay is the reciprocal of the emission rate (e^{-1}) of the level:

$$e = e_n + e_p,$$

where e_n is the electron emission rate and e_p is the hole emission rate. The emission rates themselves can be expressed as

$$e_x = B_x T^2 \exp(-\Delta E_x/kT),$$

where x is either n or p, T is the absolute temperature,

[a)]Work conducted as part of the Semiconductor Technology Program at NBS. Portions of this work were supported by DOE Task Order A021-EES and by Defense Advanced Research Projects Agency Order Number 2397.
[b)]NBS-NRC Postdoctoral Research Associate.

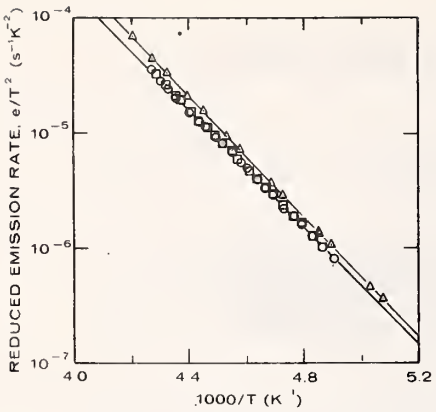

FIG. 1. Semilog plot of reduced emission rate (e/T^2) against inverse temperature for ^{34}S in n-type Si: circles, ^{34}S (Device 9); squares, ^{34}S (Device 19). Also shown is a representative plot of reduced emission rate for ^{32}S in n-type Si (triangles).

k is the Boltzmann constant, ΔE_n is the energy between the defect level and the conduction band edge, and ΔE_p is the energy between the defect level and the valence band edge. The $B_x T^2$ prefactor contains the carrier velocity, capture cross section, and the band-edge density of states. A temperature-independent cross section is explicitly assumed. It has been reported[7] that e_p for the midgap level in sulfur is much smaller than e_n so that $e \approx e_n$ and therefore the energy level of the defect is proportional to the slope of a straight line through the plot of the logarithm of (e/T^2) versus reciprocal temperature. For each device tested, 16 to 22 emission rates were measured and plotted; typical results are shown in Fig. 1. The experimental apparatus[14] and the detailed measurement technique[15] have been previously reported. The above analysis yields a value of 0.512 ± 0.002 eV below the conduction band edge for the ^{34}S deep level.[16]

The values obtained by thermally stimulated measurements for the sulfur deep level are summarized in Table I. The difference in the measured values for the sulfur deep level between the isotopes ^{32}S and ^{34}S does not appear to be due to experimental uncertainties or beam contamination. The isothermal transient capacitance measurements are able to resolve the difference in the measured energy levels, as is seen in Fig. 1. Additionally, it is highly improbable that additional impurities that may have been introduced during implantation would be responsible for the shift observed. As an illustration, nickel has an isotope that in its doubly charged state would produce a mass interference with the implantation of ^{32}S and not with ^{34}S; however, nickel is an unlikely beam contaminant and the abundance of the isotope required (^{61}Ni) is only 1.08%.[8] This argument is strengthened by the previously cited agreement between the value of the sulfur deep level obtained for implantation-predeposited ^{32}S [6] and that obtained for thermally diffuses sulfur[7] (which is 95% ^{32}S).

For these reasons, the existence of an isotope shift

TABLE I. Measured values for the sulfur deep level. The indicated uncertainties represent one standard deviation in the fit of the slope e/T^2 versus $1000/T$. The values for the energy level for all the measured devices of each type fell within the indicated range.

Thermally diffused 95% ^{32}S (Ref. 7)	Implantation predeposited ^{32}S (Ref. 6)	Implantation predeposited ^{34}S (this work)
$E_c - 0.528$ ± 0.004 eV	$E_c - 0.526$ ± 0.002 eV	$E_c - 0.512$ ± 0.002 eV

in the sulfur deep level is viewed as being due only to the increased mass of ^{34}S over that of ^{32}S. These results therefore imply that the electronic energy levels of the sulfur deep level are strongly coupled to the lattice vibrations. The difference between the energy of the deep sulfur level between the isotopes ^{32}S and ^{34}S is 2.66%; which compares favorably with the difference in the zero point energies of the vibrations ($\propto m^{-1/2}$) of 2.98%, calculated assuming the stiffness coefficients of the oscillator remain unchanged for both isotopes. The existence of an isotope shift for impurity levels has been seen in other systems, e.g., chromium in the ruby laser[17] and in luminescence from cadmium-oxygen pairs in gallium phosphide.[18]

Prior to the present study, coupling between electronic wave functions and the lattice has been seen in silicon only for radiation-damage centers, where the existence of Jahn-Teller distortions has been implied to explain such centers as the isolated vacancy,[19] the divacancy,[20] and the phosphorus-vacancy pair.[21] It must be emphasized that radiation damage effects have been eliminated in the present study by the experimental design. The results reported here represent the first time to our knowledge that an isotope shift has been observed in a deep impurity level in silicon. The existence of this shift implies strong coupling between the electronic wave function of the sulfur deep level and the silicon lattice.

The authors gratefully acknowledge H. B. Dietrich of Naval Research Laboratory for performing the implantations, Y. M. Liu for fabricating the diodes, and R. Y. Koyama and M. G. Buehler for useful discussions.

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Appendix C

Surface Preparation Procedures for Radial Profiling (Objective 3.1)

C-1 The Surface Preparation

The surface preparations chosen for study were two forms of chem-mechanical polishing and two forms of mechanical polishing. One of the chem-mechanical polishes employed premixed colloidal silica in water with a pH having been adjusted to about 10.5; it is the same material as was previously used for chem-mechanical polishing in [C-1]. The second chem-mechanical polish employed precipitated silica purchased in powder form which was then mixed with water to form a suspension, in which the pH was adjusted to about 10.5 with ethylene diamine. Because of rapid settling of this suspension, new batches were prepared daily. The two mechanical polishes were based on diamond premixed in nonaqueous fluid, one using 0.5-μm diamond, the other using 3-μm diamond. Polycrystalline man-made diamond was chosen because of uniformity of particle size and shape and prolonged retention of cutting edges. For the two lowest resistivity silicon specimens tested, 0.3-μm alumina in water was also tested as a polishing agent; this was abandoned because of excessive noise in measurement results. For the diamond processes, polishing was done against a nonwoven cloth, sold under such names as Pellon and Kempad; the colloidal silica polishing was done against a suede-like synthetic material. In both cases, the polishing cloths were bonded to a glass plate. The polishing machine used was a small tub polisher with eccentric orbital motion — an instrument commonly used for laboratory preparation of spreading resistance specimens and chosen for applicability to common practice. The load on the specimens during polishing was applied by the dead weight of a 580-g (1-1/4-lb) piston in a stabilizing collar (fig. C-1).

The diamond polishing process, as implemented for tests on the high resistivity *n*-type specimens, utilized just enough diamond slurry to dampen the polishing cloth and leave a moist appearance when distributed over the surface of the cloth. Since some of the slurry adheres to the silicon specimen and mounting block and is lost when the specimen is removed and cleaned, renewal with four to six drops of slurry after polishing two or three specimens was found necessary. Early tests on polishing used generous amounts of diamond slurry such that a layer of slurry perhaps 0.5 mm thick covered the polishing cloth. Specimen surface quality obtained when using such large amounts of slurry was inferior to that obtained with the lesser amount of slurry. Polishing cloths of the type used can be obtained from most suppliers of metallurgical polishing apparatus. However, they come in several grades intended for differing particle size abrasives, and a cloth intended for 1-μm or smaller particles should be used.

The diamond slurry used is soluble in organic solvent; cleaning of the specimens subsequent to polishing using acetone followed by methanol was found acceptable. In general, a thorough flushing appeared to remove

Figure C-1. Mounting block, piston, and collar used for top surface polishing.

the polishing residue, but a residual blue haze was seen on occasion, and it was then found necessary to swab the specimen with methanol.

Since a clear definition cannot be given to the amount of polishing which must be done with a given process to generate a surface condition fully characteristic of the process used, a reasonable but arbitrary criterion was adopted. The criterion was that at each step, a specimen was polished for 1 h or, if probe tracks were still visible after 1 h, until all previous probe tracks were removed.

Various cleaning methods and post-polishing treatments were used in conjunction with the four types of polishes. These treatments are used as subcategories to analyze the results given in subsection C-4 and are listed in table C-1. Several of these, such as the use of tap water, would not be recommended in practice. They were used, however, to test the sensitivity of the surface. Several preliminary steps such as HF stripping of oxides were tested for similar reasons.

C-2 The Specimens

The specimens used were taken from four crystals of NTD (111) silicon with nominal room temperature resistivities of 30, 65, 180, and 400 Ω·cm and from three crystals of float-zoned (111) silicon with nominal room temperature resistivities of 30, 60, and 150 Ω·cm. Although there is strong interest in NTD silicon for thyristor fabrication because of the uniformity of resistivity possible with this process, there is a need to monitor the uniformity of actual NTD material to verify that individual crystals do indeed possess the required uniformity. The present tests have therefore included float-zoned silicon with its attendant nonuniformity to test the resolution of nonuniformities possible with each of the chosen specimen preparations. To speed the polishing process, particularly the silica processes for which a specimen loading of about three pounds per square inch (psi) is preferred but difficult to obtain on the small polishing machine used, the actual specimens used were typically a quarter of a 2-in. diameter crystal slice (see fig. C-1). This gave a pressure of about 1.6 psi (11000 $N \cdot m^{-2}$). Separate specimens from each crystal were reserved for each polishing process tested.

C-3 The Probes

The probes used for the spreading resistance measurement were tungsten-osmium alloy with nominal 25 μm (1 mil) tip radius. A probe load of 25 g was used to minimize both wear and penetration. Because previous experience indicated that measurements on n-type specimens in the resistivity range being tested are strongly affected by the probes and their condition at the time of measurement in addition to the specimen surface condition [C-4], a procedure was devised to test the operating condition of the probes. For the first set of specimens, those at the lowest resistivity level, the probes were periodically checked against a stabilized 1 Ω·cm p-type specimen as is common practice for spreading resis-

Table C-1 — Description of Specimen Treatments Used in Conjunction with Polishing (Abbreviations Used in Figures and Tables Given in Left Column).

Pre-Polish Cleaning Methods

HF strip	- Immerse in electronic grade, 49% hydrofluoric acid for 2 min.
Degrease	- Immerse in 5:1:1 mixture of deionized water, hydrogen peroxide, ammonium hydroxide at 80°C for 15 min [C-1].

Post-Polishing Treatments

DI H_2O	- Flush with 18 MΩ·cm deionized water for 30 s.
DI water + detergent, or tap water + detergent	- Apply 1 or 2 drops of liquid household detergent used for dishwashing, with water as specified; scrub; rinse water as specified.
Tap water rinse	- Flush with untreated tap water for 30 s.
Scrub	- Scrub silicon surface under water with a toothbrush — generally used for detergent application.
Acet./MeOH	- Flush silicon surface with acetone, then with methyl alcohol.
Swab	- Rub silicon surface with cotton swab to remove haze left by diamond fluid or by acetone.
Blow dry	- Dry specimen for 30 s under jet of room-temperature nitrogen gas derived from boil-offf of liquid nitrogen supply.
N_2+vac. — 30 min	- Place specimen in vacuum oven, heat off, evacuate chamber to about 1/10 of an atmosphere pressure, then balance vacuum and bleed-in nitrogen to maintain about 1/4 atmosphere for 30 min.
Bake	- Bake specimen on 150°C hot plate in laboratory ambient for 15 min.
N_2+vac./Bake	- Follow procedure for N_2 + vac. - 30 min (above) except maintain oven at 150°C.

tance measurements. The probes were then cleaned and "conditioned" as necessary if they did not reproduce within ±10 percent their initial measurements on the p-type specimen. Conditioning was achieved by running the probes for several hundred measurements on a lapped silicon surface. For work on the second set of specimens, at the 60 to 65 Ω·cm level, this p-type specimen no longer appeared to be an adequate test of probe quality. Based on results obtained on 30 Ω·cm n-type silicon, a specimen of 30 Ω·cm NTD silicon, polished with 0.5-μm diamond at intervals of 2 to 3 days, was added as an extra check. For work on the remaining specimens, the probes were tested on the p-type check specimen, as above, and on a 65 Ω·cm NTD specimen polished with 0.5-μm diamond. This higher resistivity specimen provided a more severe test of probe quality than did the 30 Ω·cm specimen and appeared to serve well as a control over probe operating conditions.

C-4 Data Acquisition and Interpretation

All measurements were taken with the room darkened.

For each NTD specimen, 150 spreading resistance data were taken at probe steps of 50 μm after each preparation. The average and relative standard deviation of these data was used to estimate repeatability and signal-to-noise. For each float-zoned specimen, 150 measurements were taken after each preparation, also using 50-μm probe steps. However, the measurement response was characterized not by average spreading resistance value, but by the spreading resistance value of a particular minimum and maximum in the resistivity structure along the line scanned. For the 30 Ω·cm specimen only, a single minimum-maximum pair was chosen for analysis. For the two remaining resistivity levels of float-zoned silicon, two such pairs were chosen for analysis. Figure C-2 shows typical spreading resistance data for a float-zoned specimen and the manner in which the chosen minimum and maximum values are represented by two-ended arrows in the ensuing graphical data summary. It is noted that resistivity variations in a float-zoned specimen are generally not symmetric about a slice center. For this reason, the shape and absolute value of resistivity variation measured for separate specimens from the same crystal are not expected to be the same.

Although two types of silica polish and two grades of diamond polish were tested, the figures and tables to follow will summarize results only for the silica polish received in powdered form (and mixed as needed) and for the polish preferred overall — that using 0.5-μm diamond. Comments on the results relative to these but obtained with the premixed silica polish and the 3-μm diamond polish will be found in subsection C-7. Figure C-3 shows the repeatability of average values for NTD specimens at the 30 Ω·cm level for the two surface preparations. Figures C-4, C-5, and C-6 show the results for the 65, 180, and 400 Ω·cm NTD specimens, respectively. Figures C-7, C-8, and C-9 show the repeatability of measurement of one of the chosen structural features at the 30, 60, and 150 Ω·cm levels of float-zoned silicon, respectively. Associated with each of these figures is a table summarizing the results.

Tables C-2 through C-5 are associated with figures C-3 through C-6 for NTD specimens. Tables C-6 through C-8 are associated with figures C-7 through C-9 for float-zoned specimens. In each table, column 1 states which subset of surface conditions is used in a particular data analysis. The integers seen on the abscissa of each figure are used as "run" indices for the measurements on each specimen and are used in column 2 of each table to indicate which measurements were used for the analysis stated in column 1. For the NTD specimens (tables C-2 through C-5), column 3 gives the range of averages (of 150 data), and column 4 gives the range of relative sample standard deviations (of 150 data) associated with the runs listed in column 2. The relative sample standard deviation is the standard deviation estimated from the 150-data sample expressed as a percent of the sample mean. Consistently low values in that column indicate a surface which yields small measurement scatter. For tables C-2 through C-5, the fifth column gives the grand average of the averages (of 150 data) for the runs in question, and column 6 gives the relative sample standard deviation of the individual averages about the grand average for these runs. The smaller this value (in column 6), the more repeatable are the results for the surface preparation in question.

For the float-zoned specimens in table C-6 through C-8, the third column gives the maximum/minimum ratios for the resistivity structure feature represented in figures C-7 through C-9, respectively. The fourth column of these tables gives the corresponding maximum/minimum ratio for a second resistivity structure feature which is not illustrated in any of the figures. The maximum/minimum ratio, or some minor variation thereof, is typically used to gauge the resistivity variation due to resistivity striations. A constant value or a small range of values for this ratio (in columns 3 and 4) is indicative of a process which can give a reliable measure of resistivity variation. However, note that it is possible for a surface preparation process to allow a reliable measure of resistivity variation and at the same time give a rather poor repeatability for absolute values.

The results can be summarized as follows for all NTD specimens: specimen surfaces polished with 0.5-μm diamond gave much more repeatable R_{SP} response (average of 150 measurements) than did either type of silica-polished surface (with or without subsequent baking). Scatter within a typical set of 150 measurements on a diamond-polished specimen was nearly as small as in the best sets of data from silica-polished specimens, and it was noticeably less than the scatter in a typical set from silica-polished specimens. The only clear exceptions to the overall favorable response following diamond polishing occur for the 180 Ω·cm NTD specimen, runs 24 and 26 in figure C-5b. The two low values shown are known to have occurred immediately after changing the polishing pad. These low values may have been caused by improper loading of the fresh pad with diamond slurry, resulting in improper polishing action. It is seen from figures C-5 through C-8 and the accompanying tables that specimens polished with 0.5-μm diamond are remarkably impervious to subsequent treatment. Such specimens show little difference in

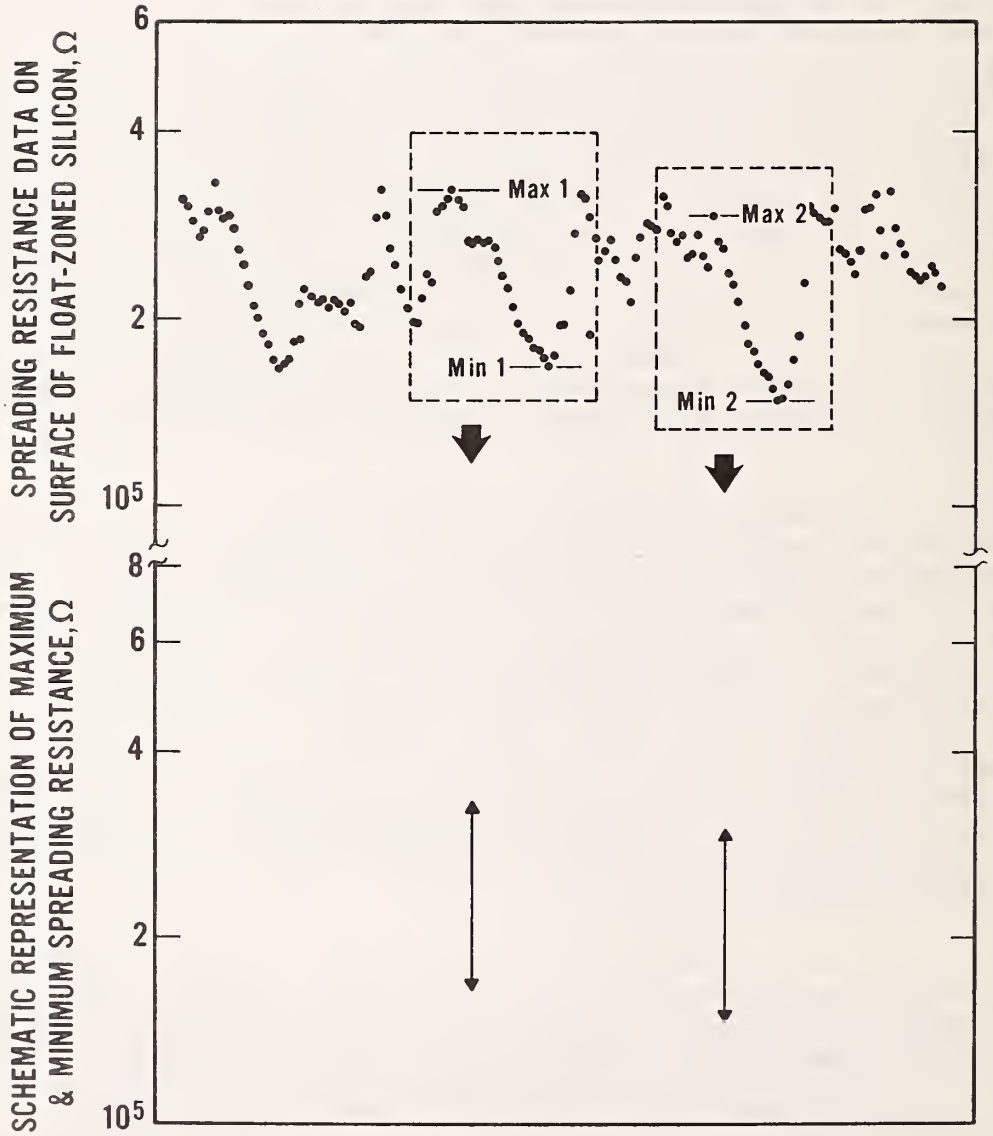

Figure C-2. Spreading resistance data from measurements on the surface of a float-zoned silicon slice illustrating manner of representation in data summary of striation structure extrema values.

Table C-2. Summary of Responses — 30 Ω·cm NTD Specimen.

Surface Condition	Runs Included	Range of Rsp Averages, Ω	Range of Pct Std Dev Individ. Runs	Grand Average Spreading Resistance, Ω	Pct Std Dev about Grand Average
Colloidal Silica Series - Figure C-3a					
Silica polish, DI H_2O rinse; blow dry: N_2 - 60 s	1, 12, 13, 14, 15	0.75×10^5 1.3×10^5	1.6 to 5.0	1.09×10^5	23
Silica polish, DI H_2O + detergent; rinse; blow dry: N_2 - 60 s	5, 9	1.31×10^5 1.35×10^5	1.8 to 4.2	1.32×10^5	2
30 min dry - vacuum chamber - N_2 flow	3, 6, 10	0.86×10^5 1.37×10^5	1.9 to 6.0	1.2×10^5	24
Bake	2, 8, 11	0.78×10^5 1.54×10^5	2.0 to 6.1	1.2×10^5	32
0.5-μm Diamond Series - Figure C-3b					
0.5-μm diamond polish Acetone/MeOH rinse; N_2 blow dry - 30 s	1, 5, 7	1.05×10^5 1.09×10^5	1.2 to 2.1	1.06×10^5	2
0.5-μm diamond polish DI H_2O + detergent or tap water + detergent rinse; N_2 blow dry - 30 s	3, 8, 10	1.06×10^5 1.12×10^5	1.6 to 1.9	1.10×10^5	3
Bake	2, 4, 6, 9	1.09×10^5 1.15×10^5	1.6 to 2.2	1.11×10^5	2.6
All surfaces starting with diamond polish	1 to 10	1.09×10^5 1.15×10^5	1.2 to 2.2	1.10×10^5	3.2

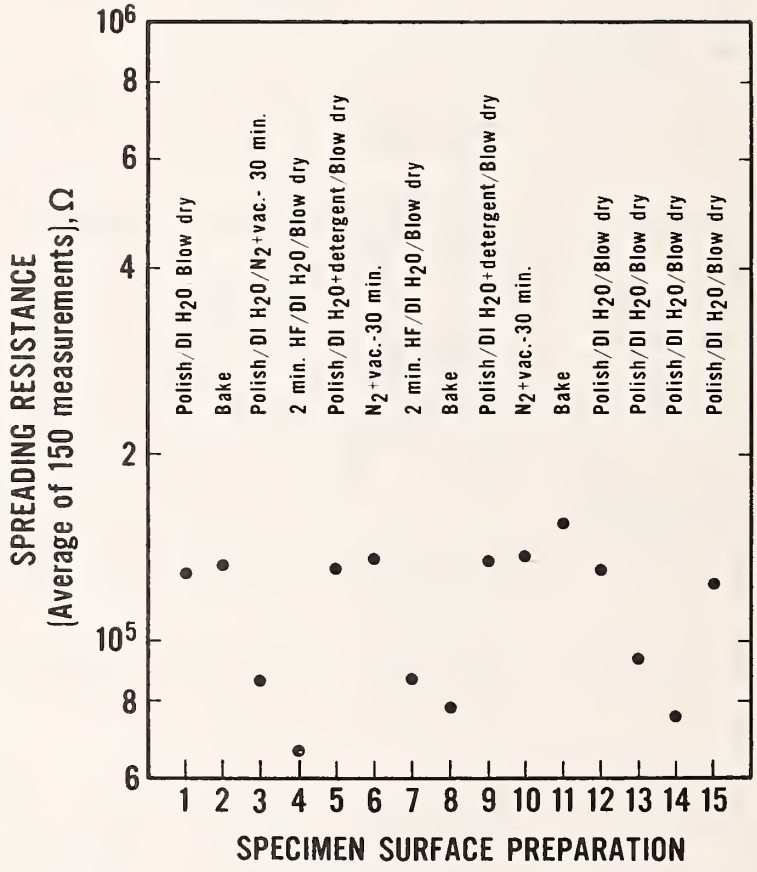

Figure C-3a. Spreading resistance average *vs.* surface preparation: colloidal silica series — 30 Ω·cm NTD silicon specimen.

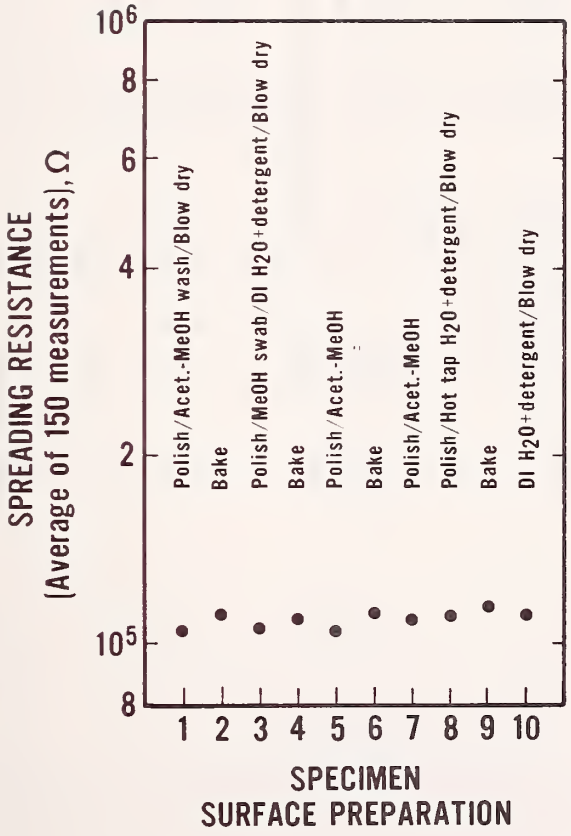

Figure C-3b. Spreading resistance average *vs.* surface preparation: 0.5-μm diamond series — 30 Ω•cm NTD silicon specimen.

Table C-3. Summary of Responses — 65 Ω·cm NTD Specimen.

Surface Condition	Runs Included	Range of Rsp Averages, Ω	Range of Pct Std Dev Individ. Runs	Grand Average Spreading Resistance, Ω	Pct Std Dev about Grand Average
Colloidal Silica Series - Figure C-4a					
Silica polish, DI H_2O rinse; blow dry: N_2 - 60 s	1, 2, 5	2.9×10^4 3.6×10^5	2.8 to 9.5	1.7×10^5	99
Silica polish, DI H_2O + detergent; rinse; blow dry: N_2 - 60 s	10, 13, 16	1.5×10^5 3.2×10^5	15 to 38	2.5×10^5	35
30 min dry - vacuum chamber - N_2 flow	3, 6, 11, 14	3.2×10^4 4.7×10^5	3.2 to 150	2.4×10^5	82
Bake	4, 7, 8, 9, 12, 15, 17, 19	7.7×10^4 5.2×10^5	2.6 to 23	3.1×10^5	56
0.5-μm Diamond Series - Figure C-4b					
0.5-μm diamond polish Acetone/MeOH rinse; N_2 blow dry - 30 s	9, 15, 19, 20	2.25×10^5 2.60×10^5	1.7 to 2.0	2.3×10^5	7
0.5-μm diamond polish DI H_2O + detergent or tap water + detergent rinse; N_2 blow dry - 30 s	11, 13, 17	2.28×10^5 2.44×10^5	1.3 to 2.4	2.35×10^5	3.8
Bake - after diamond polishing only	10, 12, 14, 16, 18	2.2×10^5 2.7×10^5	1.3 to 4.8	2.5×10^5	8
All surfaces starting with diamond polish	9 to 20	2.2×10^5 2.7×10^5	1.3 to 4.8	2.4×10^5	6.7

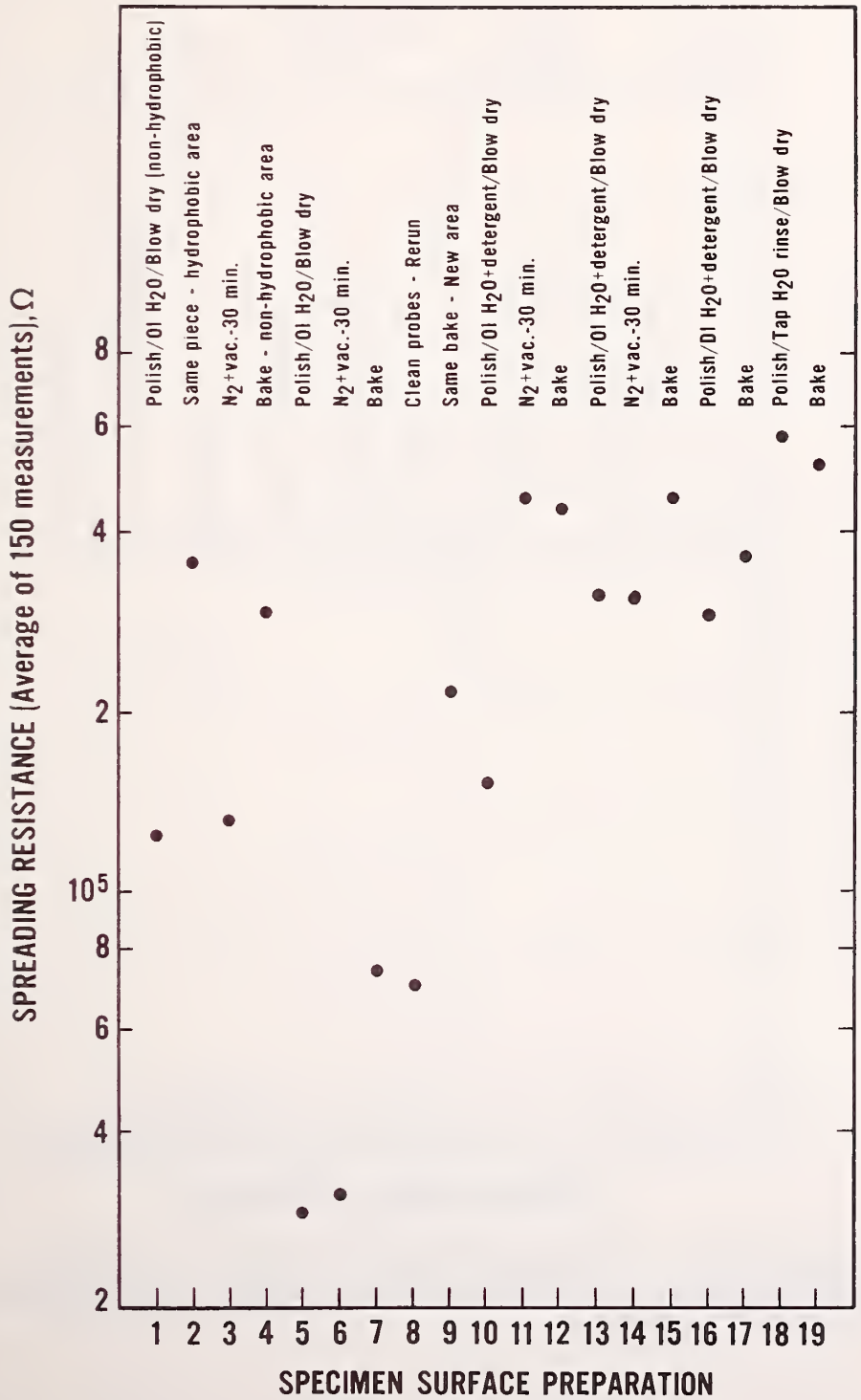

Figure C-4a. Spreading resistance average *vs.* surface preparation: colloidal silica series — 65 Ω·cm NTD silicon specimen.

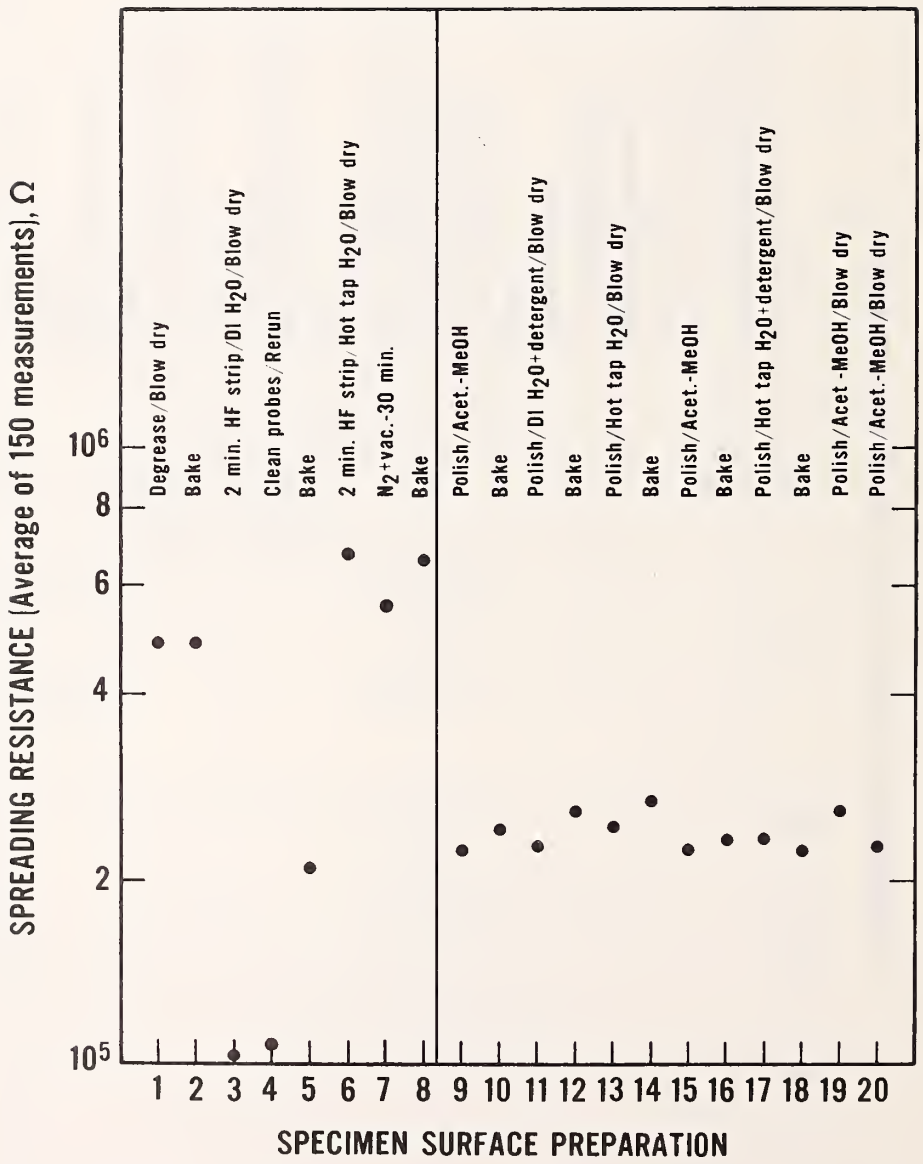

Figure C-4b. Spreading resistance average *vs.* surface preparation: 0.5-μm diamond polish series — 65 Ω•cm NTD silicon specimen.

Table C-4. Summary of Responses — 180 Ω•cm NTD Specimen.

Surface Condition	Runs Included	Range of Rsp Averages, Ω	Range of Pct Std Dev Individ. Runs	Grand Average Spreading Resistance, Ω	Pct Std Dev about Grand Average
Colloidal Silica Series - Figure C-5a					
Silica polish, DI H_2O rinse; blow dry: N_2 - 60 s	1, 4, 18, 19 21, 23	4.8×10^5 1.2×10^6	2.4 to 18	7.8×10^5	33
Silica polish, DI H_2O + detergent; DI rinse; blow dry: N_2 - 60 s	7, 10, 13, 14	3.2×10^5 1.3×10^6	5.2 to 16	9.2×10^5	47
30 min dry: vacuum chamber + N_2 flow	2, 5, 8, 11	5.1×10^5 1.6×10^6	2.5 to 5.5	9.5×10^5	52
Bake - hot plate	3, 6, 9, 12, 15 17	6.0×10^5 2.2×10^6	2.0 to 11	1.1×10^6	50
Bake: vacuum + N_2 flow	20, 22, 24	2.1×10^5 5.1×10^5	*3.0 to 7.0	3.8×10^5	39
0.5-μm Diamond Series - Figure C-5b					
0.5-μm diamond polish Acetone/MeOH rinse; blow dry: N_2 - 30 s	9, 15, 19, 20, 21	5.9×10^5 6.40×10^5	1.4 to 2.6	6.1×10^5	2.9
0.5-μm diamond polish DI H_2O + detergent or tap water + detergent; rinse; blow dry: N_2 - 60 s	11, 17, 20	6.4×10^5 6.7×10^5	1.1 to 2.6	6.5×10^5	2.4
0.5-μm diamond polish Acetone/MeOH/Di H_2O + detergent; rinse; blow dry: N_2 - 60 s*	28, 30, 32, 34	5.8×10^5 6.3×10^5	1.6 to 5.4	6.1×10^5	3.0
Bake - after diamond polishing only*	10, 12, 14, 16, 18, 23, 29, 31, 33, 36, 38, 40	6.3×10^5 7.6×10^5	1.6 to 6.0	7.0×10^5	4.9
All surfaces starting with diamond polish	7 to 40	5.9×10^5 7.6×10^5	1.1 to 6.0	6.6×10^5	7.5

*Runs 24, 25, 26, and 27 were not included. Erratic results seen for runs 24 and 26 followed replacement of the polishing pad. It is believed the pad was not properly loaded with diamond for these runs.

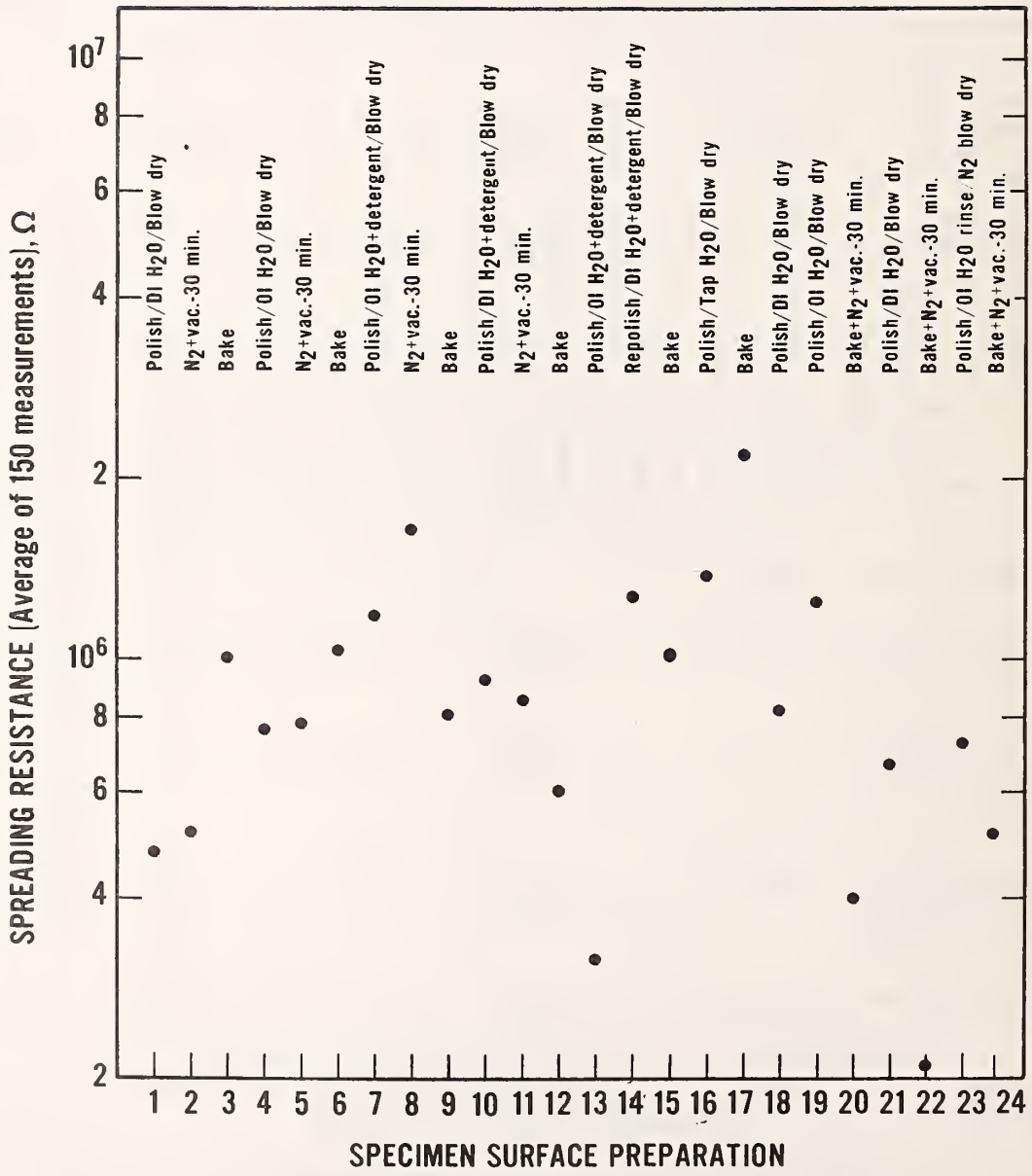

Figure C-5a. Spreading resistance average *vs.* surface preparation: colloidal silica series — 180 Ω·cm NTD silicon specimen.

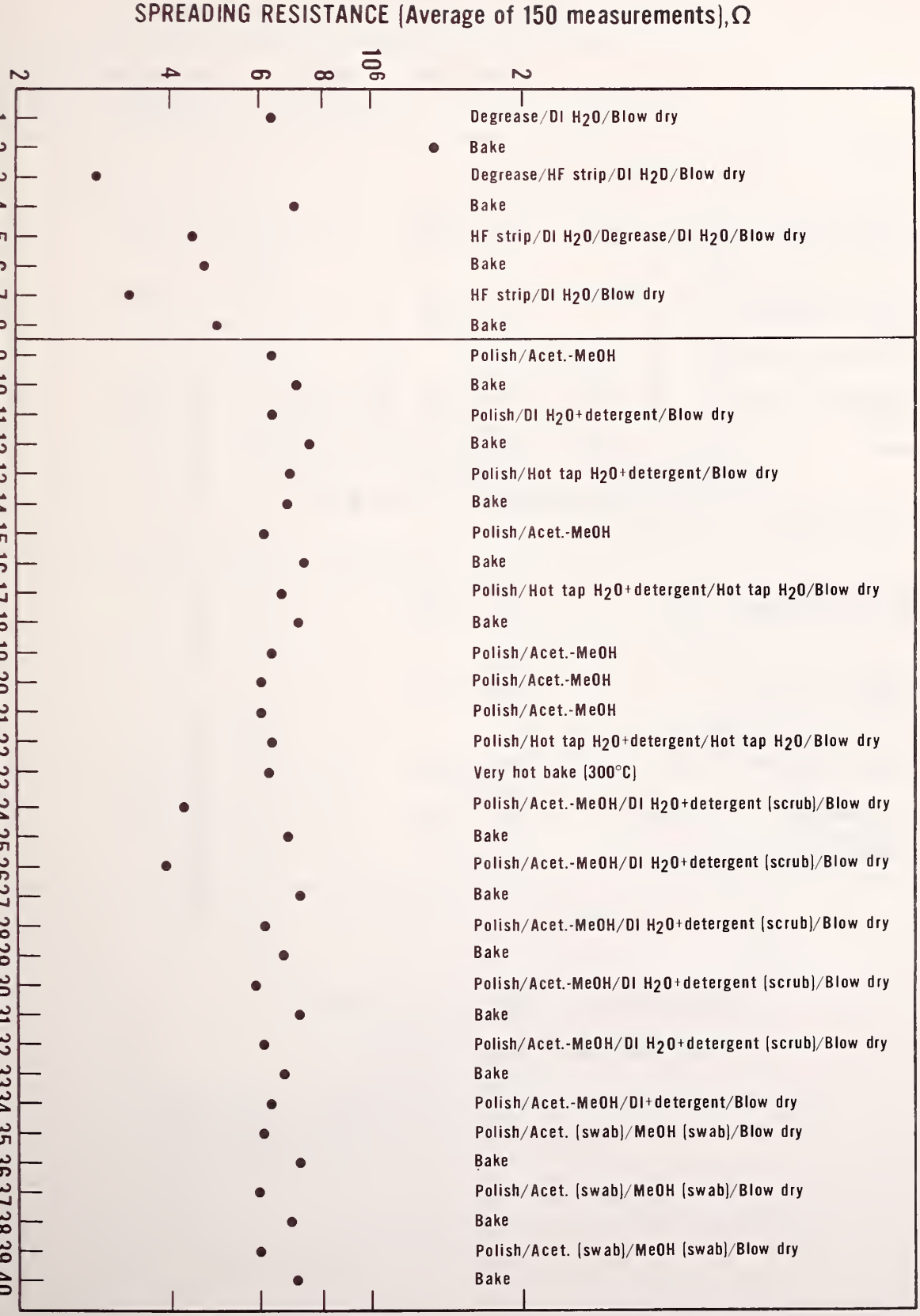

Figure C-5b. Spreading resistance average *vs.* surface preparation: 0.5-μm diamond polish series — 180 Ω·cm NTD silicon specimen.

Table C-5. Summary of Responses - 400 Ω·cm NTD Specimen.

Surface Condition	Runs Included	Range of Rsp Averages, Ω	Range of Pct Std Dev Individ. Runs	Grand Average Spreading Resistance, Ω	Pct Std Dev about Grand Average
Colloidal Silica Series - Figure C-6a					
Silica polish, DI H_2O rinse; blow dry: N_2 - 60 s	1, 4, 7, 10	3.4×10^5 1.7×10^6	1.4 to 5.5	8.6×10^5	69
Silica polish, DI H_2O + detergent rinse; blow dry: N_2 - 60 s	13, 15	6.1×10^5 1.0×10^6	13 to 14	8.3×10^5	38
30 min dry: vacuum chamber + N_2 flow	2, 5, 8, 11	4.3×10^5 2.0×10^6	1.1 to 2.9	9.4×10^5	78
Bake	3, 6, 9, 12, 14, 16	1.4×10^6 2.4×10^6	1.9 to 4.4	1.7×10^6	25
0.5-μm Diamond Series - Figure C-6b					
0.5-μm diamond polish Acetone/MeOH rinse; N_2 blow dry	8, 14, 18, 19, 20	9.1×10^5 9.3×10^5	1.7 to 2.7	9.2×10^5	1
0.5-μm diamond polish DI H_2O + detergent; rinse; blow dry: N_2 - 30 s	10, 12	8.8×10^5 9.3×10^5	1.7 to 1.8	9.0×10^5	4.5
Bake - after diamond polishing only	9, 11, 13, 15, 17	9.2×10^5 1.05×10^6	2.5 to 3.8	1.0×10^6	6.0
All surfaces starting with diamond polish	8 to 20	8.8×10^5 1.05×10^6	1.7 to 3.8	9.5×10^5	5.8

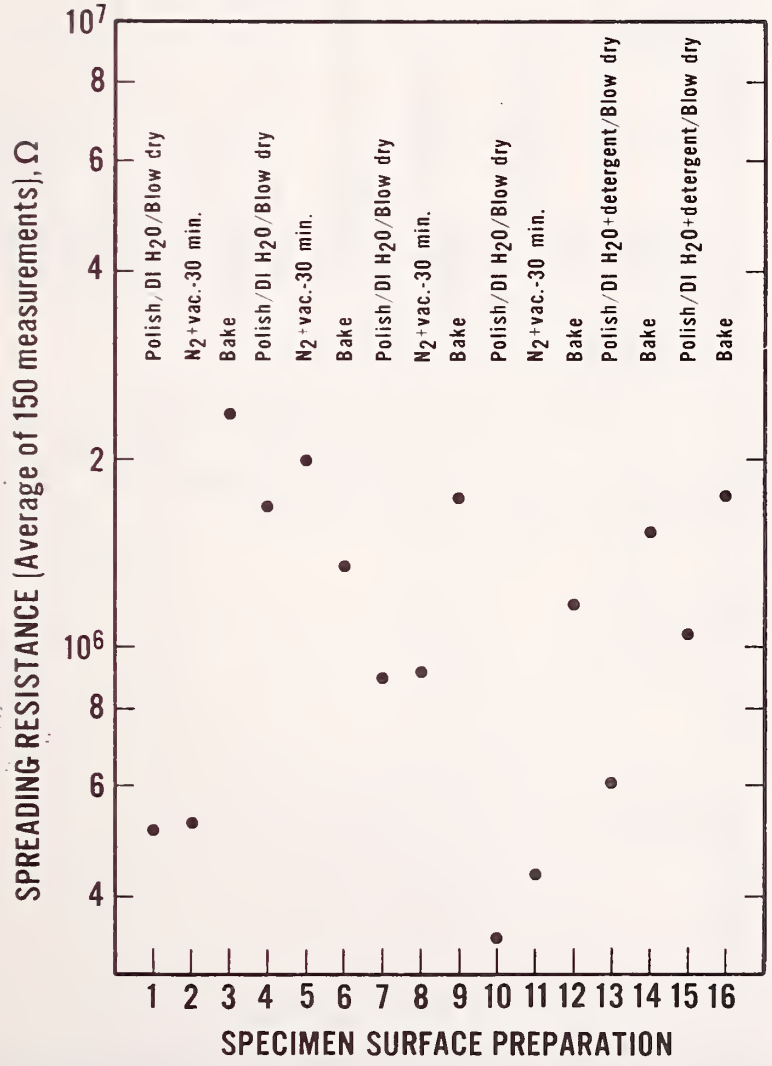

Figure C-6a. Spreading resistance average *vs*. surface preparation: colloidal silica series — 400 Ω•cm NTD silicon specimen.

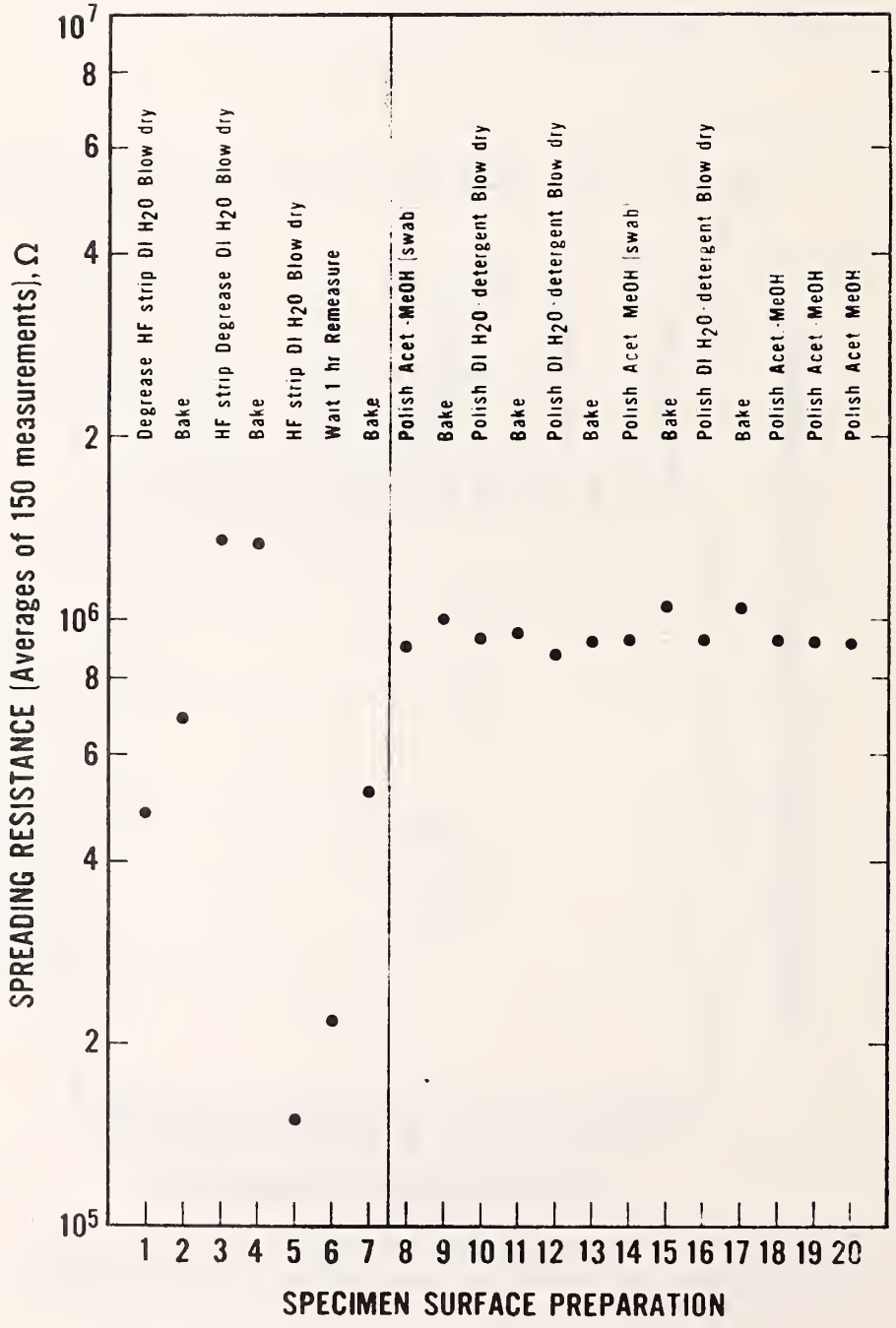

Figure C-6b. Spreading resistance average *vs*. surface preparation: 0.5-μm diamond polish series — 400 Ω•cm NTD silicon specimen.

Table C-6. Summary of Response — 30 Ω·cm Float-Zoned Specimen.

Surface Condition	Runs Included	Max/Min Ratio 1st Feature	Max/Min Ratio 2nd Feature
Colloidal Silica Series - Figure C-7a			
Silica polish, DI H_2O rinse; Blow dry: N_2 - 60 s	1, 11, 12	1.3 to 1.54	not done - this specimen
Silica polish, DI H_2O + detergent; Rinse; Blow ery: N_2 - 60 s	5, 8	1.31 to 1.42	not done - this specimen
30-min dry: vacuum chamber - N_2 flow	3, 6, 9	1.32 to 1.39	not done - this specimen
Bake	2, 7, 10	1.35 to 1.39	not done - this specimen
0.5-μm Diamond Series - Figure C-7b			
0.5-μm diamond polish; Acetone/MeOH rinse; Blow dry: N_2 - 30 s	1, 5, 8, 9	1.54 to 1.64	not done - this specimen
0.5-μm diamond polish; MeOH rinse DI H_O + detergent; Rinse; Blow dry: N_2 - 60 s	3	1.56	not done - this specimen
Bake	2, 4, 7	1.57 to 1.64	not done - this specimen

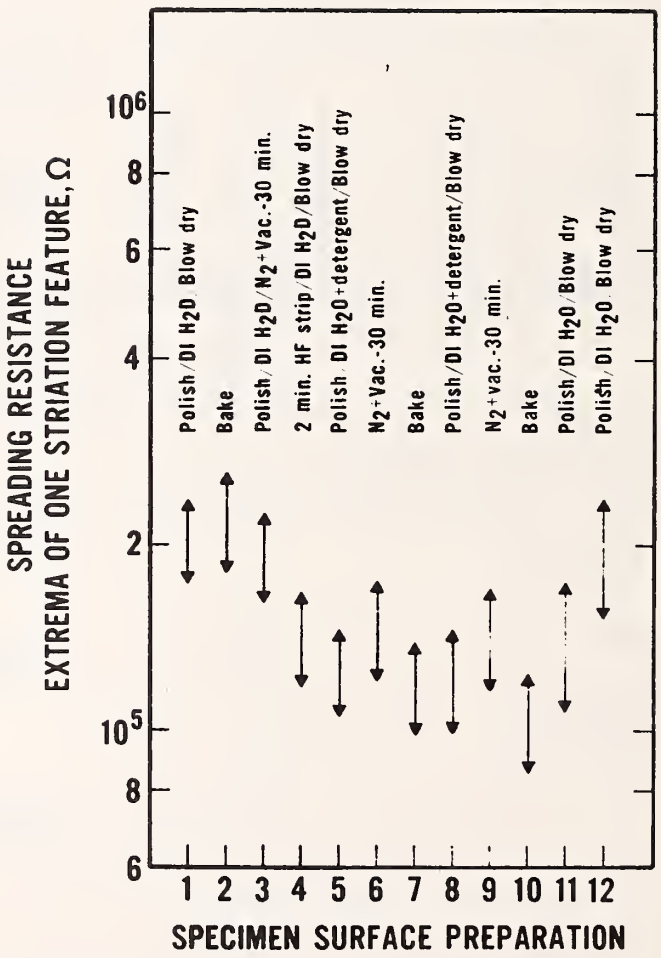

Figure C-7a. Spreading resistance maximum and minimum *vs*. surface preparation for one resistivity striation feature: colloidal silica series — 30 Ω•cm float-zoned silicon specimen.

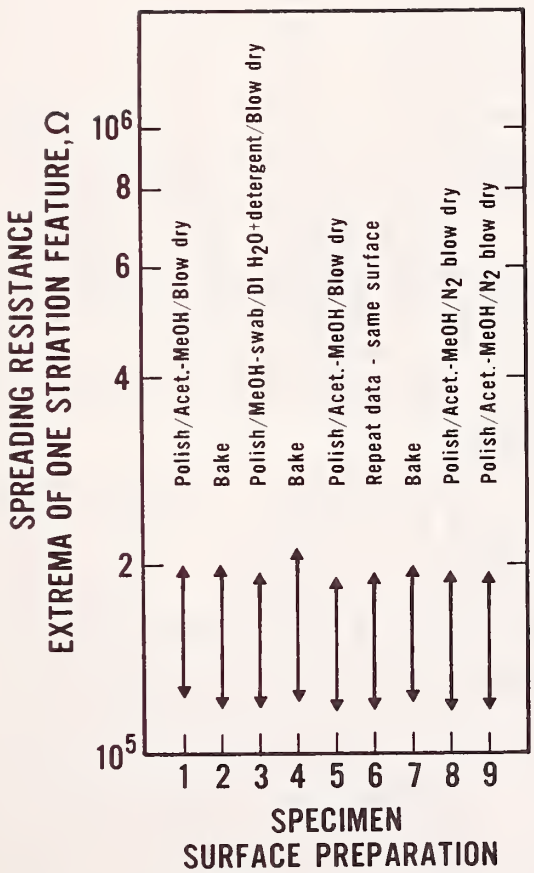

Figure C-7b. Spreading resistance maximum and minimum *vs.* surface preparation for one resistivity striation feature: 0.5-μm diamond polish series — 30 Ω·cm float-zoned silicon specimen.

Table C-7. Summary of Response — 60 Ω·cm Float-Zoned Specimen.

Surface Condition	Runs Included	Max/Min Ratio 1st Feature	Max/Min Ratio 2nd Feature
Colloidal Silica Series - Figure C-8a			
Silica polish; DI H_2O rinse; Blow dry: N_2 - 60 s	1, 4	2.0 to 2.3	1.64 to 1.67
Silica polish; DI H_2O + detergent; Rinse; Blow dry: N_2 - 60 s	7, 10	2.25 to 2.46	1.8 to 2.06
30 min dry: vacuum chamber + N_2 flow	2, 5, 8	2.01 to 2.73	1.68 to 2.10
Bake	3, 6, 9, 11	2.11 to 2.77	1.82 to 2.16
0.5-μm Diamond Series - Figure C-8b			
0.5-μm diamond polish; Acetone/MeOH rinse; Blow dry: N_2 - 30 s	8, 14, 18, 19, 20, 21	1.82 to 1.91	1.51 to 1.71
0.5-μm diamond polish; Acetone/MeOH rinse; Blow dry: N_2 - 30 s	8, 14, 18, 20, 21	1.82 to 1.91	1.64 to 1.71
0.5-μm diamond polish; DI H_2O + detergent or tap water + detergent; rinse; Blow dry: N_2	10. 12, 16	1.82 to 1.92	1.67 to 1.77
Bake	9, 11, 13, 15, 17	1.87 to 2.14	1.60 to 1.78

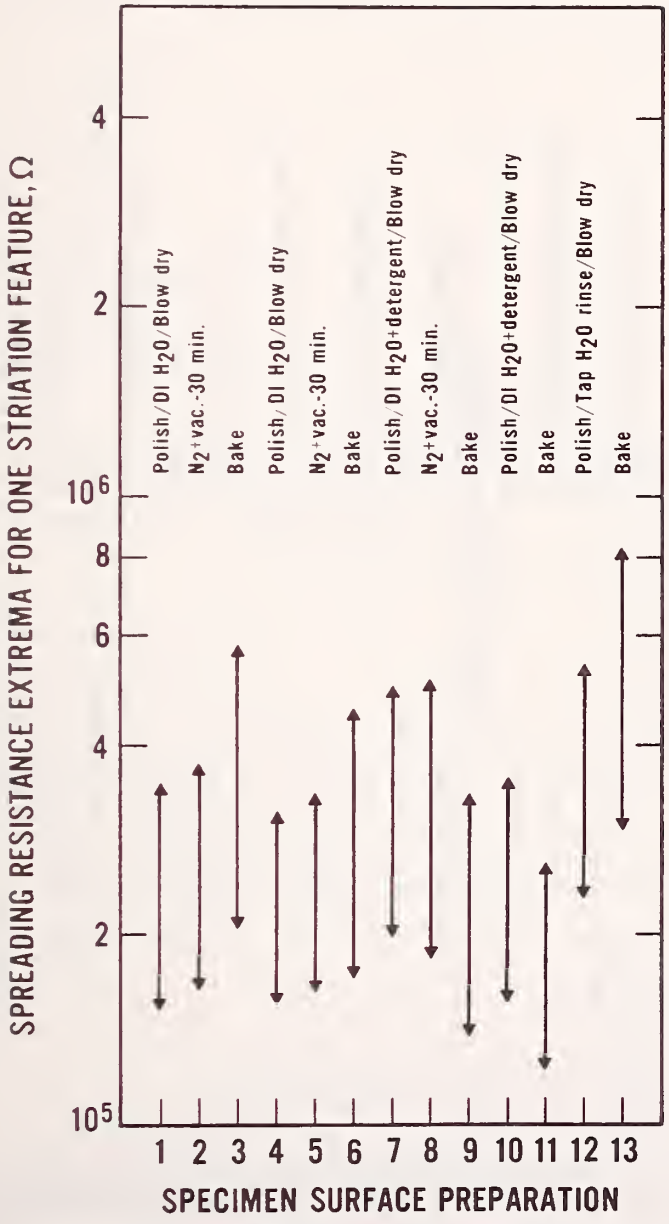

Figure C-8a. Spreading resistance maximum and minimum *vs*. surface preparation for one resistivity striation feature: colloidal silica series — 60 Ω·cm float-zoned silicon specimen.

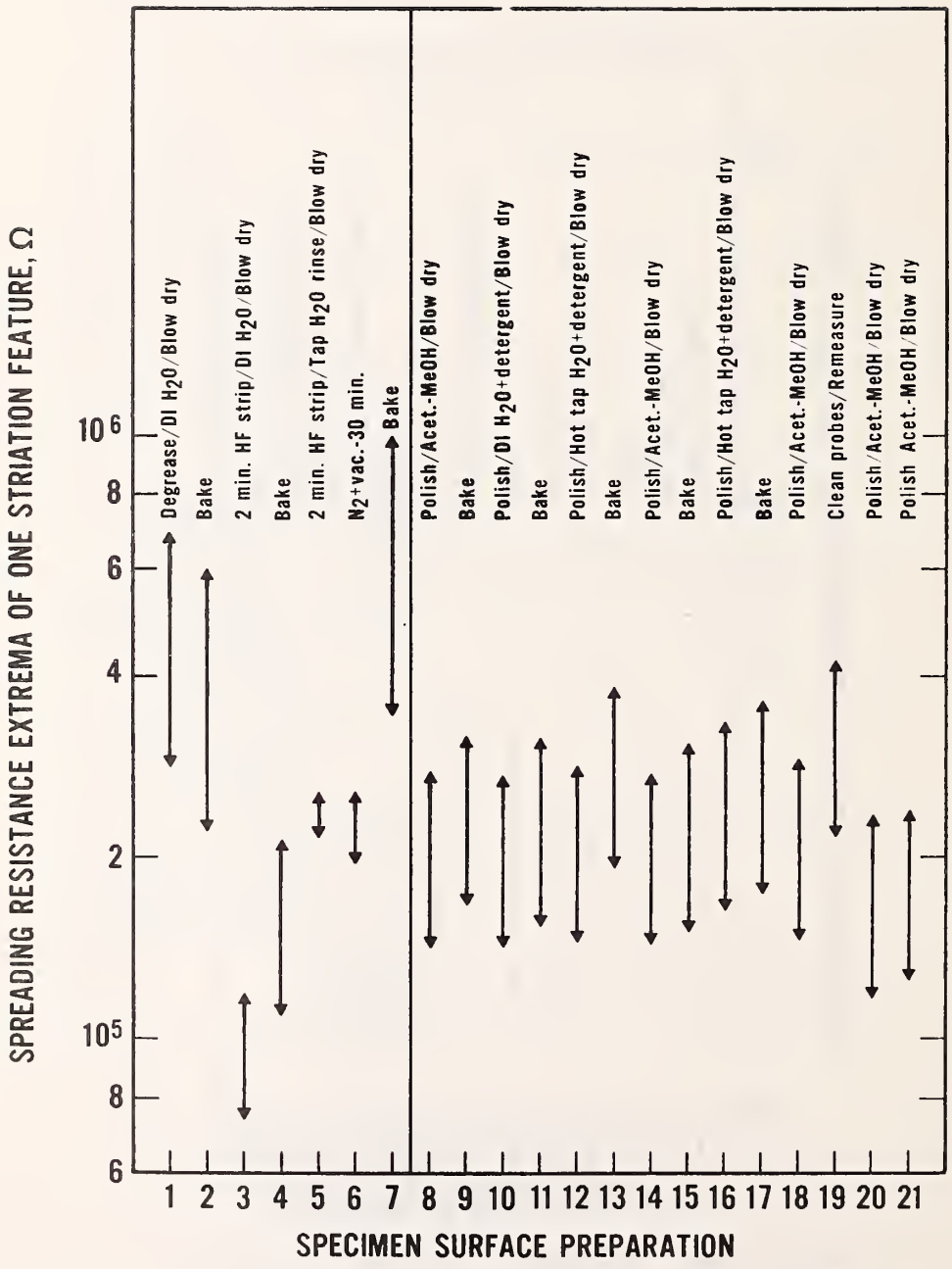

Figure C-8b. Spreading resistance maximum and minimum *vs.* surface preparation for one resistivity striation feature: 0.5-μm diamond series — 60 Ω•cm float-zoned silicon specimen.

Table C-8. Summary of Response — 150 Ω·cm Float-Zoned Specimen.

Surface Condition	Runs Included	Max/Min Ratio 1st Feature	Max/Min Ratio 2nd Feature
Colloidal Silica Series - Figure C-9a			
Silica Polish; DI H_2O rinse; Blow dry: N_2 - 60 s	1, 4, 16	1.61 to 1.90	1.49 to 1.79
Silica Polish; DI H_2O + detergent; Blow dry: N_2 - 60 s	7, 9, 12	1.77 to 1.87	1.61 to 1.78
30 min dry: vacuum chamber + N_2 flow	2, 5, 10	1.54 to 1.84	1.44 to 1.74
Bake	3, 6, 9, 11, 13, 15	1.55 to 1.89	1.51 to 1.74
0.5-μm Diamond Series - Figure C-9b			
0.5-μm diamond polish; Acetone/MeOH rinse; Blow dry: N_2 - 30 s	7, 13, 17, 18, 19	1.82 to 1.93	1.68 to 1.85
0.5-μm diamond polish; DI H_2O + detergent or tap water + detergent; Blow dry: N_2 - 60 s	9, 11, 15	1.80 to 1.93	1.88 to 1.89
0.5-μm diamond polish; Acetone/MeOH rinse; DI H_2O + detergent scrub; rinse; Blow dry: N_2 - 60 s	20, 22, 24	1.83 to 2.01	1.84 to 1.94
Bake	8, 10, 12, 14, 16, 21, 23, 25	1.90 to 2.15	1.69 to 2.05

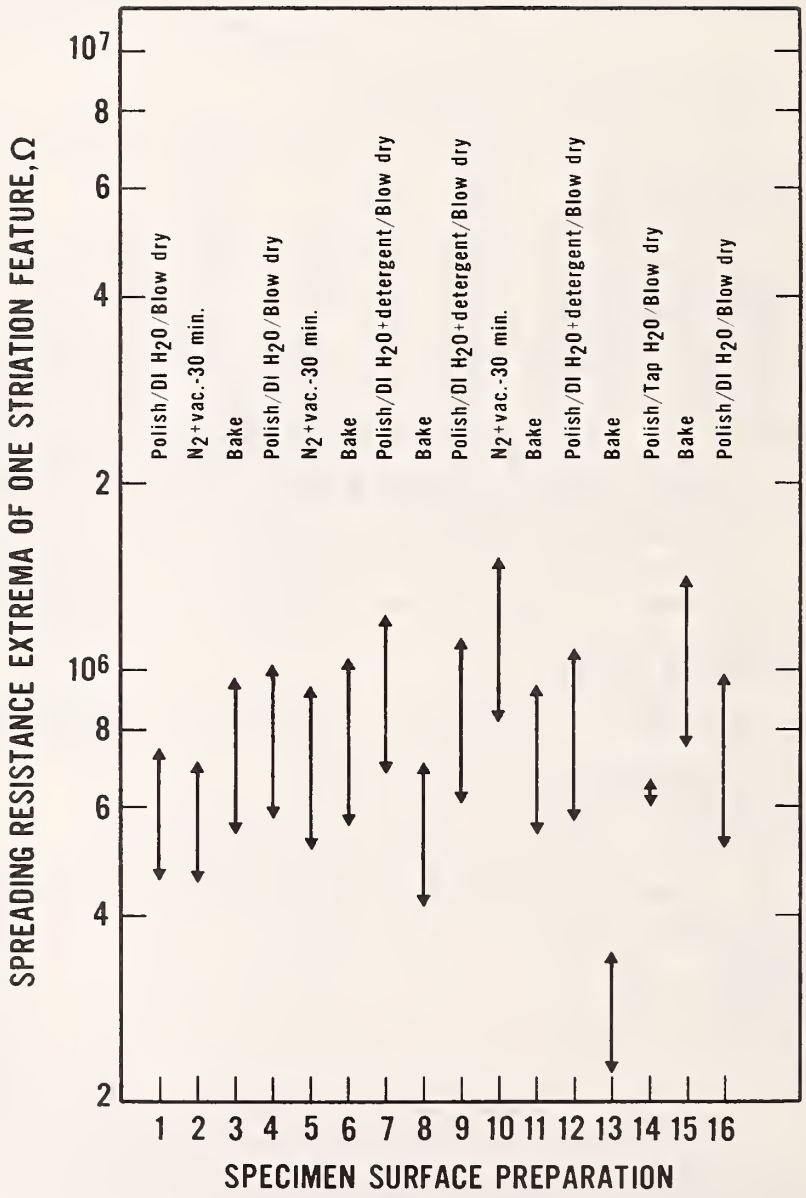

Figure C-9a. Spreading resistance maximum and minimum *vs.* surface preparation for one resistivity striation feature: colloidal silica series — 150 Ω·cm float-zoned silicon specimen.

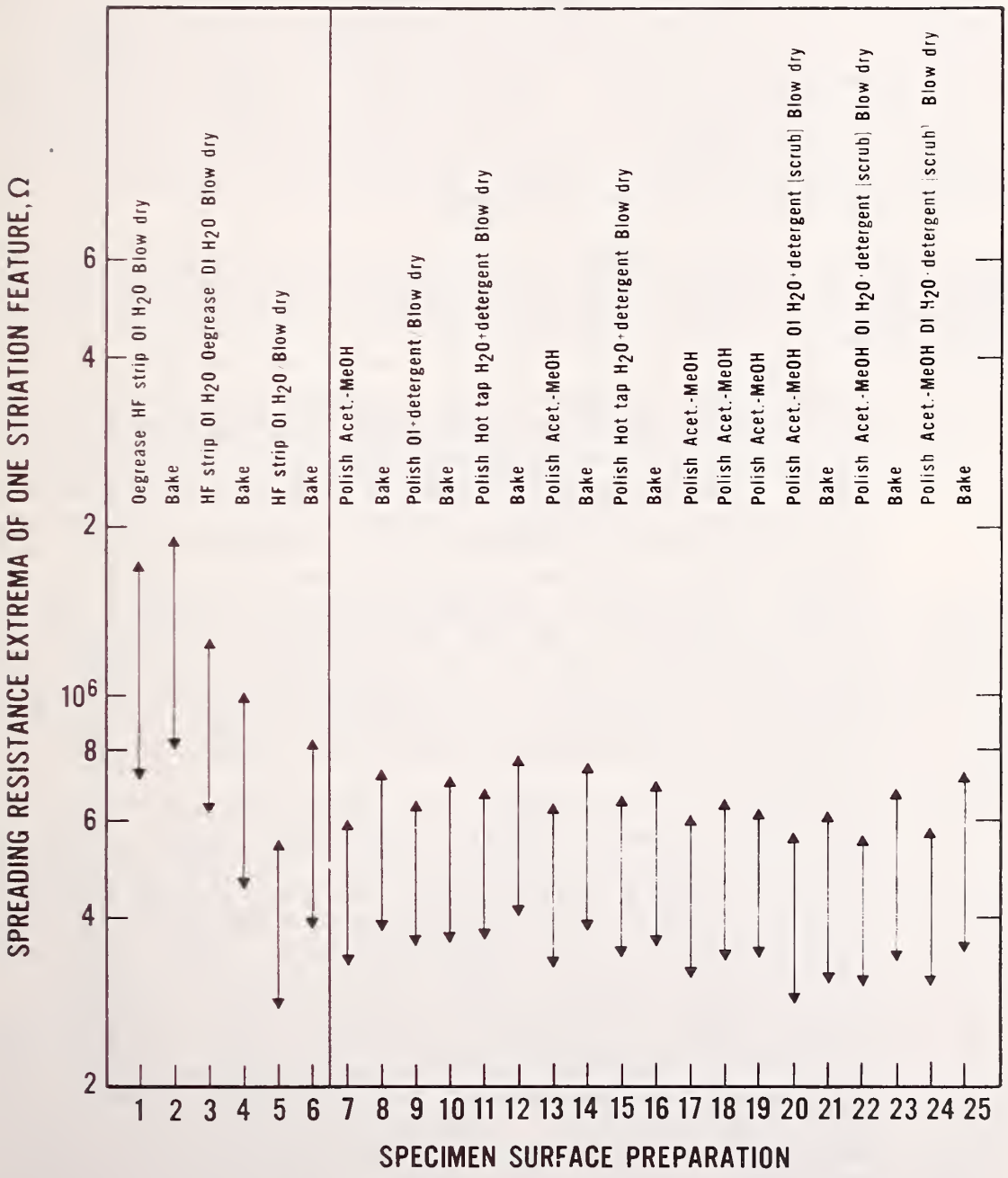

Figure C-9b. Spreading resistance maximum and minimum *vs.* surface preparation for one resistivity striation feature: 0.5-μm diamond polish series — 150 Ω•cm float-zoned silicon specimen.

average spreading resistance, whether cleaned with organic solvents, acetone and methanol, or with water (deionized or tap) plus a liquid kitchen detergent. The only post-polishing treatment having a measurable effect was baking; the same 15-min baking at 150°C normally used following silica polishing caused an increase in spreading resistance of about 5 to 15 percent when used following diamond polishing. However, the baking step after diamond polishing does not further improve the measurement repeatability for high resistivity n-type specimens. Moreover, as shown in section C-1, diamond polishing alone gives acceptably repeatable measurements for the full spectrum of (111) n-type and (111) p-type resistivity values. Baking following a 0.5-μm diamond polishing, therefore, appears to be an unnecessary operation.

In comparison with the results illustrated in figures C-3 through C-6 and tables C-2 through C-5 for the NTD silicon, the following behavior was generally obtained with premixed colloidal silica and with 3-μm diamond polishing:

1. Polishing with premixed silica suspension gave results which were somewhat more reproducible than those obtained with mix-as-needed silica suspension and reported in the figures and tables. However, even the premixed silica gave a scatter of 12 to 28 percent of individual averages about the grand average (increasing with specimen resistivity) for NTD specimens which had been rinsed with deionized water and blown dry. For measurements following a subsequent baking of specimens, this scatter increased to as much as 65 percent. The relative sample standard deviation for 150 data points on a specimen polished with the premixed silica was somewhat better than obtained with the other silica polish but did not have the consistently low value obtained with 0.5-μm diamond polish.

2. Polishing with 3-μm diamond gave measures of repeatability which were as good as obtained with 0.5-μm diamond polishing for all but the 400 Ω•cm NTD specimen. For this specimen, the relative standard deviation about the grand average degraded to about ±10 percent. The relative sample standard deviation of 150 data points was only slightly worse following 3-μm diamond polishing (typically ±3 percent) than was found following 0.5-μm diamond polishing (typically ±2 percent). However, average spreading resistance measured on 3-μm diamond-polished specimens was somewhat higher than on the 0.5-μm polished specimen of the same resistivity. This difference increased with increasing resistivity: 5 percent for the 35 Ω•cm specimens to 40 percent for the 400 Ω•cm specimens. Also, the difference in measurement average between baked and freshly polished specimens was nearly twice as large for the 3-μm diamond-polished specimens as it was for the 0.5-μm polished specimens. Finally, as was the case for specimens polished with 0.5-μm diamond, no advantage in terms of reduced scatter or improved repeatability was found to result from baking of specimens subsequent

to polishing with 3-μm diamond. The overall relative merits of 0.5- and 3-μm diamond-polished surfaces will be discussed in section C-7.

For the float-zoned specimens, as illustrated in figures C-7 through C-9, much better repeatability of absolute R_{SP} values for striation maxima and minima is obtained from diamond-polished specimens than is obtained from silica-polished specimens. This is consistent with the results found for average R_{SP} values on NTD specimens. Also, as can be seen from the figures and from tables C-6 through C-8, the repeatability of maximum/minimum ratios is also better for the diamond-polished specimens. The same relative changes, due to cleaning or baking of specimens after polishing noted above for NTD specimens, also were obtained for float-zoned specimens. There are two principal points demonstrated by the data on float-zoned specimens. First, diamond polishing can be used to obtain a reliable measure of both absolute and relative radial resistivity variation. Second, silica polishing can also give a reasonably reliable measure of relative resistivity variation (although not as good a measure as obtainable from diamond-polished specimens), but absolute values of individual features measured on such specimen surfaces are not acceptably repeatable.

C-5 Temporal Stability of 0.5-μm Diamond-Polished Specimens

An experiment was run to estimate the temporal stability of (111) n-type silicon specimens when polished with 0.5-μm diamond. Temporal stability refers to the period of time over which a specimen, once polished, will give the same measurement result. Specimens of 65, 180, and 400 Ω·cm NTD silicon were polished with 0.5-μm diamond in nonaqueous fluid, rinsed with acetone and methanol, and blown dry. Fifty spreading resistance measurements were taken and the measurements repeated at intervals up to 30 days. The probes were checked against a separate piece of 65 Ω·cm (111) NTD silicon freshly polished each time with 0.5-μm diamond, as well as against the standard 1 Ω·cm p-type specimen. For each sequence of measurements, the probes were required to give average spreading resistance values on these probe-check specimens within ±10 percent of target values. Probe cleaning and conditioning were done as necessary to achieve target values. Variations with time on the 65 Ω·cm temporal stability test specimen were up to ±10 percent for the first 48 h and appeared to be no worse for up to 30 days. Variations on the 180 Ω·cm specimen were up to 15 percent for the first 2 days and 18 percent for 30 days. Variations for the 400 Ω·cm specimen were up to 18 percent for the first 2 days and up to 25 percent for 30 days. Changes of measured spreading resistance with time were nearly always towards increasing spreading resistance values, as is the case if the same specimens are baked following diamond polishing. However, it was found that the increase due to aging is larger than that due to baking, at least for the 180 and 400 Ω·cm specimens. Since these tests were limited, the results should be considered only indicative. In particular, much other spreading resistance data were taken during the course of the stability study, and probes were reconditioned many times, with gradual but no-

ticeable change in their contact shape. It must be remembered that changes in measured spreading resistance values can be due to two factors: changes in the specimen and changes in the probes. Since the primary means of verifying probe quality at each step of the stability test utilized a 65 Ω·cm NTD specimen, the factor due to probe change was minimized at this resistivity. It is therefore reasonable for the total variation to be less at the 65 Ω·cm level than at the higher resistivities. Earlier results [C-4] indicated that (111) *n*-type specimens which were nonaqueously mechanically polished (with aluminum oxide) had a strong sensitivity to the specific nature of the probes.

The question of temporal stability is important in two situations. The first occurs when the specimen of interest cannot be measured immediately after polishing. The second relates to measurement calibration where it may be difficult to repolish all specimens immediately prior to taking calibration data, for example, when calibration data are taken frequently or when calibration specimens are not mounted on a composite block. In either respect, it is useful to compare the possible error encountered in this resistivity range of *n*-type silicon as a result of measuring an "old" diamond-polished surface with the uncertainty caused by nonrepeatability of freshly polished silica surfaces as seen in tables C-2 to C-5. The data indicate that even "old" diamond-polished surfaces give more reliable measurements than do fresh silica-polished surfaces.

C-6 Effect of Load on Colloidal Silica Polishing

As noted in subsection C-2, the polishing machine used for specimen preparation was operated with about 1.6 psi on the specimen, which is less than the pressure recommended (∿3 psi, 21000 $N \cdot m^{-2}$) for optimal stock removal rate with silica polishing. It was decided, therefore, to test the effect on the repeatability of spreading resistance measurements of silica polishing with polishing pressures of 3 psi. For this test, a production-quality slice polisher was employed. Polishing was done with the colloidal silica which was obtained in powdered form, and the polishing cloth was the same suede-texture material used with the small laboratory scale machine. To minimize multiple replication of the polishing procedure, replication was simulated by use of six sequentially sliced 180 Ω·cm NTD specimens, which were caustic-etched subsequent to sawing; one level of repolishing was done. Figure C-10 summarizes the averages of 40 spreading resistance measurements taken on each slice as polished and after baking. For purposes of comparison, measurements at probe loads of both 25 g and 45 g are shown. Much better repeatability was obtained with the 45-g load than with the 25 g load on the freshly polished specimens. However, the overall data distribution for silica-polished specimens measured at 45 g is not quite as good as was obtained at 25 g on the 0.5-μm diamond-polished 180 Ω·cm specimen shown in figure C-5. Moreover, when the silica-polished specimens were baked, even the 45-g data had a noticeably wider distribution than was shown in figure C-5 for the diamond-polished specimens. Data taken at 25 g, whether on silica-polished only or on silica-polished and baked

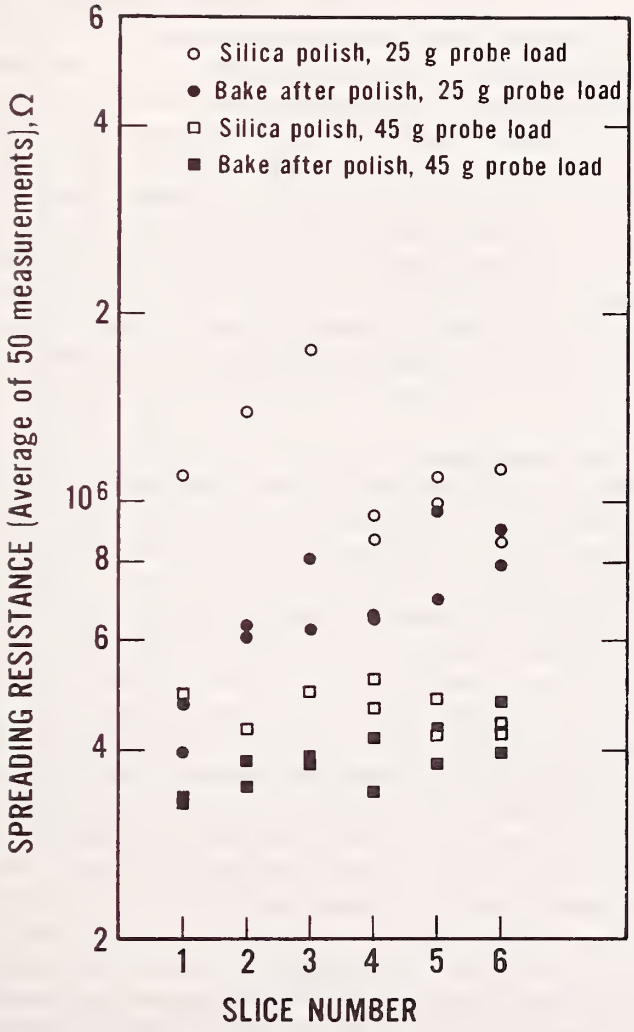

Figure C-10. Repeatability of average spreading resistance values for six equivalent 180 Ω•cm NTD silicon slices polished with colloidal silica on large machine.

specimens, show considerably more scatter than the data from the diamond-polished specimens.

C-7 Discussion of Results

For the NTD specimens, both improved repeatability of average spreading resistance (R_{SP}) value and decreased scatter within a set of measurements result from polishing with 0.5-μm diamond. The cause of increase in average R_{SP} values following baking of a diamond-polished specimen is not understood. Note, however, that the increase is of the same order, 5 to 15 percent, depending on the resistivity level, whether the specimens were washed with acetone-methanol or with water (DI or tap) plus a detergent. Although it is possible that the methanol first used had absorbed some water and that the measurement change following baking results from dehydration of the surface, the same shift was generally observed when fresh bottles of methanol were used. The effect of baking after diamond polishing on temporal stability was not studied. Since no advantage in terms of reduced measurement scatter or improved repeatability is found to result from baking following diamond polishing, this extra step following polishing appears to be dispensable.

For the float-zoned specimens, much more repeatable absolute R_{SP} values are obtained with diamond polish than with silica polish. However, while the range of maximum/minimum ratios in the bottom portion (0.5-μm diamond polish) of tables C-6 through C-8 is better than the range in the top portion (silica polish) of those tables, it is not as much better as might be expected from the results on the NTD specimens. However, three factors distinguish the measurements and calculated results on NTD specimens from those on float-zoned specimens. The first is related to the fact that the structures chosen for study on the float-zoned specimens have very sharp maxima and minima. As a result, each maximum or minimum was formed by one or two data points (fig. C-2). Statistically, it is much harder to reproduce the value of a single point than it is to reproduce an average value, as in the case of the NTD specimen analysis. The second factor is due to the dopant microsegregration phenomenon, which is responsible for the observed resistivity striations in float-zoned material [C-5], both across the diameter of a crystal, or slice, and down its length. Since different specimen depths were interrogated with successive polishing steps, small changes in the exact size and shape of the resistivity structures of interest are expected to result, with consequent effect on the repeatability of the values measured. The third factor simply relates to the propagation of variance for a ratio, as was used to characterize repeatability of measurement on the float-zoned specimens. If the relative standard deviations of the maximum and minimum values used in the ratio are the same, then the relative standard deviation of the ratio is $\sqrt{2}$ times this value.

Despite these distinctions between NTD and float-zoned specimens, it is clear from the improved repeatability of both absolute R_{SP} values and ratios of striation feature that *diamond polishing gives the user*

much greater confidence in measurement results on float-zoned as well as on NTD silicon.

Based on the results for both NTD and float-zoned specimens, polishing with diamond offers clear advantages for obtaining highly repeatable, low noise spreading resistance measurements on (111) n-type silicon in the resistivity range studied. This range, 30 to 400 $\Omega \cdot$cm, is of primary interest to producers of power control semiconductor devices. Both grades of diamond gave measurements with acceptably low scatter and high repeatability of average value for top surface measurements of bulk specimens. The difference in average spreading resistance as a function of diamond particle size noted in section C-4 probably relates to different observed amounts of surface damage to the silicon. However, if the different damage levels affect the measurement through the metal semiconductor barrier phenomenon [C-2,C-3], the relative results from the two types of diamond might well depend on the probe set used [C-4]. Any choice between the two diamond grades tested must be made based on factors not evidenced in the data presented in section C-4. The choice made is based primarily on the desire to apply the advantages evident for high resistivity n-type layers to depth profiles of thyristor structures. To do this, it is necessary to utilize a process which is acceptable over a wide range of resistivities of both p- and n-type silicon. Previous experience indicated that to obtain data with low scatter on low resistivity silicon, such as found in the emitter layers of thyristors, a smooth specimen surface is preferable. Such a surface is more nearly obtainable with 0.5-μm diamond than with 3-μm diamond, since a much higher scratch density is being encountered with the 3-μm diamond than with the 0.5-μm diamond. This higher scratch density also makes it difficult to judge the quality of the probe contact from the damage pattern left in silicon.

Because of reduced scratch damage and ease of judging probe quality, polishing with 0.5-μm diamond is considered the preferred specimen preparation for high resistivity n-type specimens when the higher polishing speed of 3-μm diamond is not mandated and as the starting point for improved thyristor profiling. Figure C-11 shows a photomicrograph of a typical silicon surface obtained using the recommended process.

Suppliers of diamond compound, other than the one used for these tests, may use fluids which are not so readily soluble in acetone or methanol, and cleaning procedures should be tested for the slurry chosen. Final cleaning using distilled water plus detergent or even tap water plus detergent gave results which are virtually indistinguishable from those obtained on acetone-methanol-cleaned specimens. Despite these results, use of water soluble organic fluids, which are also available for diamond slurries, should probably be avoided unless verified independently for quality of resulting measurements.

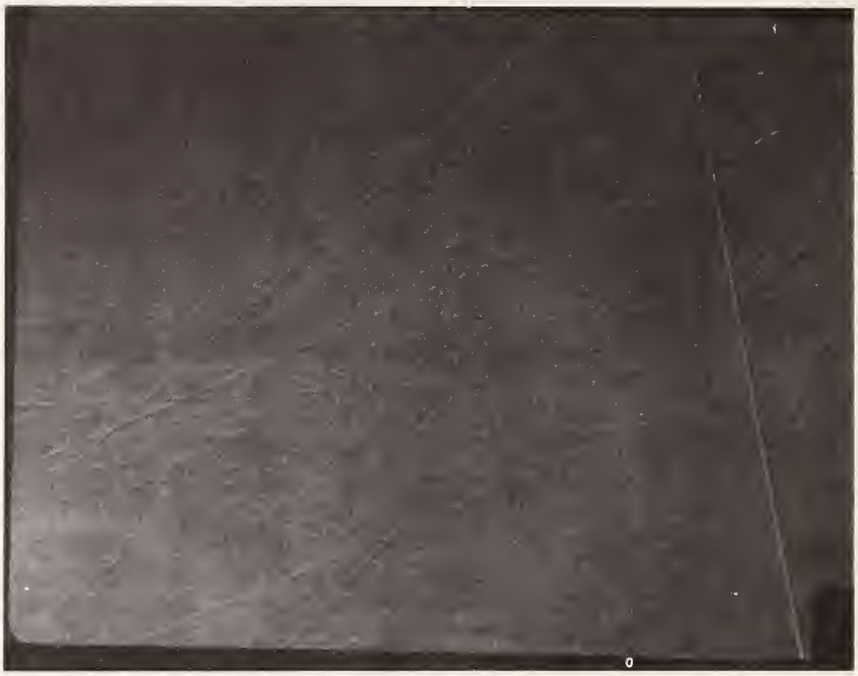

Figure C-11. Photomicrograph of silicon slice after polishing with 0.5-μm diamond (220X magnification).

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Appendix D

Depth Profiling Using the Preferred Surface Preparation (Objective 3.2)

D-1 Introduction

Diamond polishing, just demonstrated to be advantageous for top surface spreading resistance measurements, was examined for application to bevel sectioning prior to spreading resistance depth profiling of thyristor device structures. It is important to test whether the use of diamond causes detrimental effects in the interpretation of p-type layers or of highly doped n-type layers which would offset the advantage of repeatability just seen for lightly doped n-type layers. Before such tests could be made, two preliminary tests on bulk specimens were required. The first was a study of the effect on spreading resistance measurements of diamond polishing of bulk specimens against frosted glass; the second was a comparison of the effects of diamond polishing and colloidal silica polishing on the spreading resistance measurements of a full range of calibration specimens.

D-2 Preliminary Tests

The first test is required because a modification of the diamond process used for top surface polishing is necessary for bevel sectioning. For top surface polishing, the specimen is polished against a reasonably soft and therefore mechanically compliant polishing cloth. For large area specimens, deformation of the cloth is minimal, and only modest edge rounding of the specimen is observed. However, beveling for depth profiling involves only a small area of specimen surface, on the order of 25 mm^2, with a resulting deformation of the polishing cloth under the specimen much too large to obtain a flat beveled surface which intersects sharply with the specimen top surface. Tests were therefore made of other surfaces which could be used for specimen beveling in conjunction with diamond and which would give acceptably flat specimen surfaces. Previous experience indicated greatly increased occurrence of specimen edge fracture and damage to the work surface when single stage polishing is done at the steep angles (5 to 10 deg) normally used for full thyristors. Therefore, all initial tests of diamond beveling discussed below were made at bevel angles of 1 deg 9 min. Such an angle might well be used for detailed information about the relatively shallow cathode emitter.

The first process tested used 0.5- and 1-μm diamond prebonded to films of plastic, 0.12 mm (3 mils) thick. The films were, in turn, backed with adhesive which was used to attach the films to a glass plate. Despite tests with three different lubricants, the specimen-beveled surfaces were much more heavily scratched than were the specimen top surfaces polished with the same grade of diamond (in slurry form) when using the compliant polishing cloth. Moreover, beveled surfaces were rounded, indicating that even this thin a plastic film was compressing too much under the load of the specimen. Next, the same 0.5-μm

diamond in nonaqueous fluid used for top surface polishing was tested against a fresh glass plate. Extreme damage was seen on the silicon-beveled surfaces, most often caused by edge chipping of the silicon. This chipping was believed due to difficulties in maintaining an adequate lubricating film between the silicon and the glass plate. Finally, the same 0.5-μm diamond slurry was used, but the polishing was done against a piece of glass plate which had been prefrosted with 9-μm aluminum oxide. The resulting beveled surfaces had scratch densities which were about comparable with those obtained with diamond bonded to plastic: less than obtained with fresh glass plate but more than obtained for top surface polishing. However, the beveled surface was flat, as determined by surface profilometer, and if a reciprocating instead of orbital motion was used during beveling, a very uniform density of scratches could be obtained (see fig. D-1).

Tests were then made of the effect of this increased surface damage (beveled surface damage compared with top surface damage) on spreading resistance measurement response. Twelve bulk silicon specimens were selected at the approximate resistivity levels 0.001, 0.01, 0.1, 1, 10, and 400 Ω·cm for both (111) n-type and (111) p-type. The top surface of each was polished with 0.5-μm diamond in the usual manner with a soft polishing cloth. Then the specimens were mounted for beveling at 1 deg 9 min using 0.5-μm diamond and a frosted glass plate. Fifty measurements were taken along a line perpendicular to the intersection of the two surfaces, half the measurements being on each surface. Changes in spreading resistance values measured on the two surfaces of a specimen ranged from a few percent to 25 percent. Since this large a change was considered unacceptable, the tests were halted before all specimens were tested. Tests were rerun in new areas of the test specimens, but 0.5-μm diamond was replaced by 0.1-μm diamond* (in paste form) for the beveling procedure. Again, the frosted glass plate was used. This procedure resulted in a beveled surface with a lower scratch density than resulted from use of 0.5-μm diamond but generally higher than found on the specimen top surfaces. Spreading resistance measurements exhibited shifts less than 5 percent when crossing from beveled to top surface. Therefore, this process (0.1-μm diamond polishing) was chosen as the procedure to test diamond beveling for depth profiling. As before, acetone followed by methanol is used to clean polishing residues. Figure D-2 shows a typical surface beveled with 0.1-μm diamond on a frosted glass plate.

To test the effect of diamond polishing on spreading resistance calibration, a multichip composite calibration block which included both n- and p-type specimens with (111) orientation was assembled in a manner previously described [D-1]. Two other composite blocks, one for each conductivity type, were also used in conjunction with silica polishing. Table D-1 gives the resistivity values of the silicon chips on the three

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*UB 1/10 Diamond Paste (0.1-μm diamond) from the Glennel Corporation, West Chester, PA, was found satisfactory for this purpose.

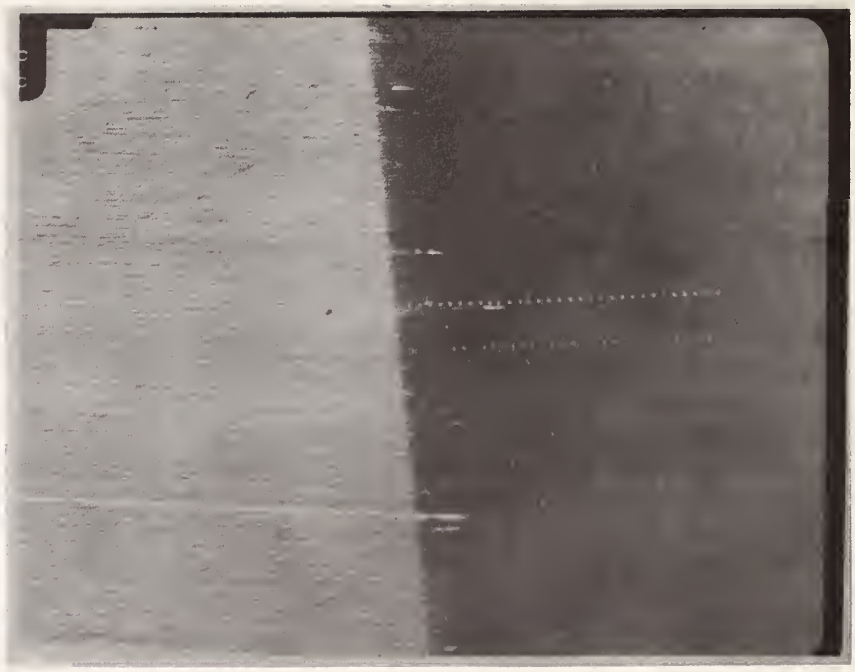

Figure D-1. Photomicrograph of silicon specimen beveled with 0.5-μm diamond against ground glass. Top surface was polished with 0.5-μm diamond against soft cloth.

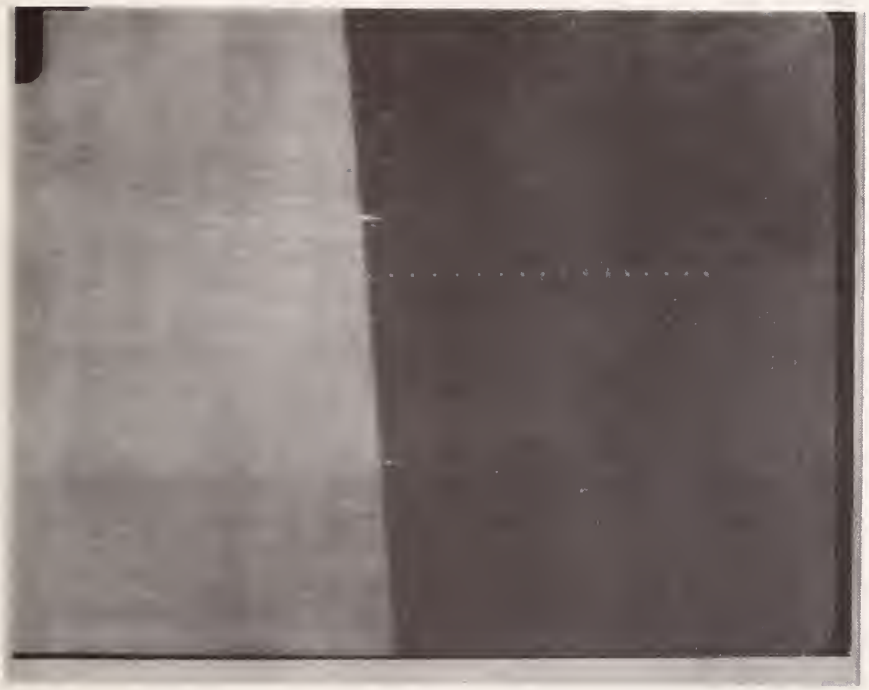

Figure D-2. Photomicrograph of silicon surface beveled with 0.1-μm diamond against ground glass. Top surface was polished with 0.5-μm diamond against soft cloth.

Table D-1. Composite Resistivity Block Layout.

Silica Surface Calibration		0.5-μm Diamond Surface
p-type (Ω·cm)	*n*-type (Ω·cm)	Calibration (Ω·cm)
0.000998	0.00137	0.268 (P)
0.0197	0.0335	1.28 (N)
0.693	1.28	1.69 (P)
10.4	32.0	5.17 (N)
0.0028	0.00208	28.3 (P)
0.0534	0.0491	66.0 (N)
1.69	3.03	386.0 (P)
28.3	66.0	397.0 (N)
0.0043	0.00429	0.000998 (P)
0.0936	0.0935	0.00137 (N)
2.87	5.17	0.0028 (P)
65.9	137.0	0.0021 (N)
0.0125	0.0126	0.0197 (P)
0.268	0.454	0.0126 (N)
5.71	14.8	0.0936 (P)
386.0	397.0	0.0935 (N)

composite calibrations blocks used for this test. Numerous measurements were made of the spreading resistance calibration response after 0.5-μm diamond polishing of the mixed conductivity type blocks and premixed colloidal silica polishing of the separate conductivity type blocks.

The purpose was to compare the spreading resistance measurement response on diamond polished surfaces with that on silica polished surfaces over a wide range of resistivity values of both conductivity types. From this comparison, possible areas in the resistivity spectrum for which diamond polishing gave less satisfactory results than did silica polishing could be identified. Depending on the severity of such possible unfavorable response, the advantages of diamond polishing already seen for high resistivity n-type silicon might be negated for purposes of depth profiling.

Results of calibration measurements for silicon surfaces polished with 0.5-μm diamond and with colloidal silica are shown in figure D-3 for n-type specimens and in figure D-4 for p-type specimens. Data points in the figures are connected by line segments for ease of visualization only. Since previous work [D-1,D-2] clearly indicates that thermal treatment (baking) is preferred following aqueous medium (colloidal silica) polishing for p-type silicon, only data from such a surface are compared with diamond polishing data for p-type. However, since the preferability of baking following aqueous medium (silica) polishing has not been clear for (111) n-type silicon, measurements on both types of surfaces are compared with diamond-polished specimen data for n-type specimens. Data are shown for two different times in the life of the probes; those shown in figures D-3a and D-4a were taken about four weeks before the rest, and at a time when only a 1 Ω•cm p-type specimen was used for checking probe quality. A 65 Ω•cm NTD specimen, described in section 3.3.1.3, and a 0.001 Ω•cm p-type specimen were used as additional checks of probe quality prior to acquisition of data shown in all other parts of figures D-3 and D-4. A limited amount of data taken with a second set of probes is shown for both n- and p-type specimens.

The general agreement between calibration data obtained on diamond-polished p-type specimens and on silica-polished and baked specimens is quite good. However, two differences are noted. Diamond-polished specimens at the lowest resistivity values (below 0.1 Ω•cm) generally yield higher spreading resistance values than do the comparable specimens which were silica polished and baked. Diamond-polished specimens also appear to manifest little, if any, of the nonlinearity in the vicinity of 0.1 Ω•cm which is found on the silica-polished specimens and attributed to a metal-semiconductor barrier at the contact [D-3,D-4]. The difference in calibration for low resistivity p-type specimens is generally of little consequence for thyristors, since it occurs for a dopant level ($>10^{19}$ atm•cm^{-3}) not generally found in thyristor diffusions and not found in any of the thyristors tested in section D-4. The difference in p-type calibration data for the two surface types in the vicinity of 0.1 Ω•cm is not large but is taken as a manifestation of slightly different contact mechanisms on the two types of p-type surfaces.

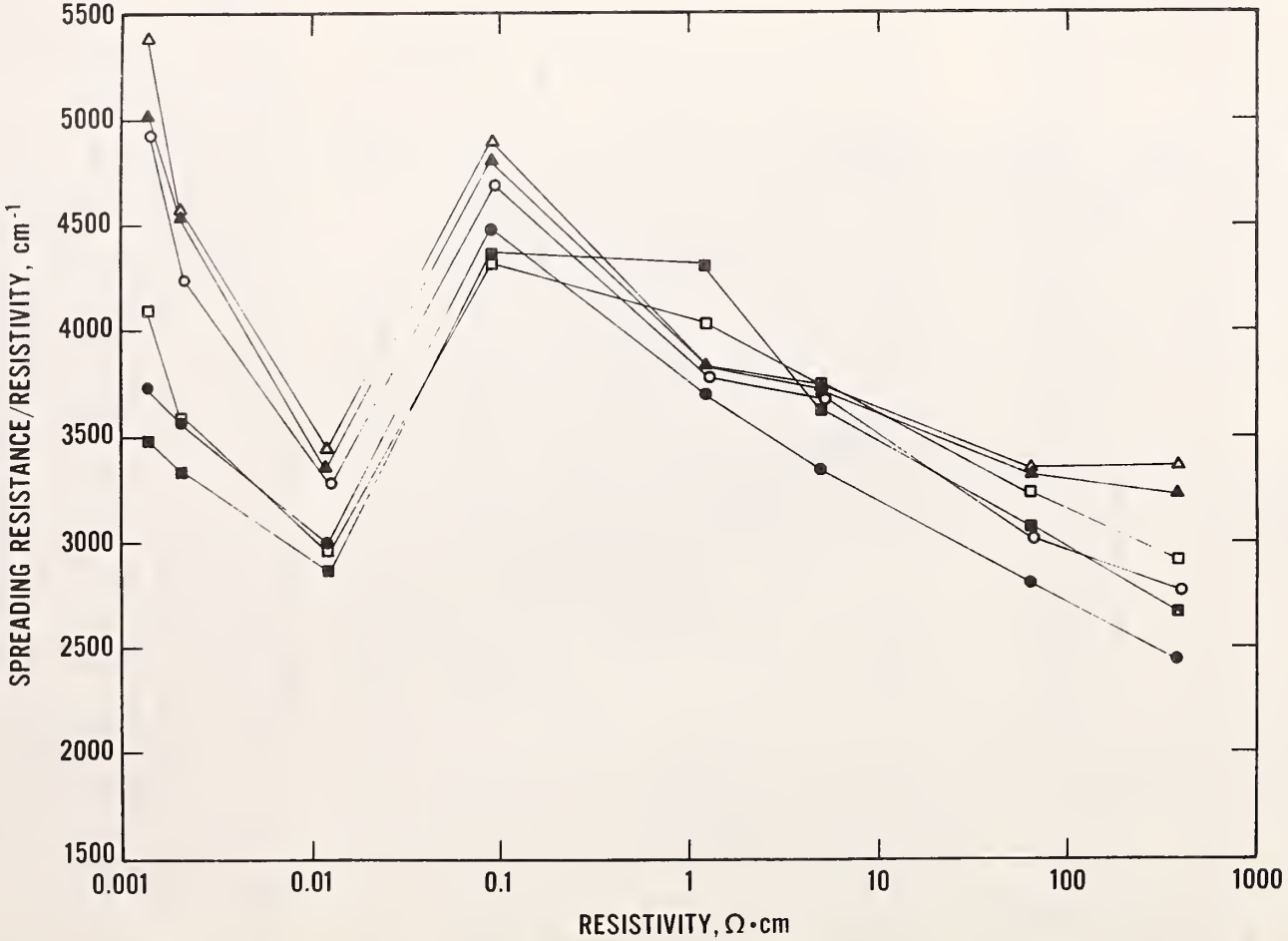

Figure D-3a. Calibration response for (111) n-type silicon polished with 0.5-μm diamond — probe set A (probe quality checked at mid-range resistivity only). Measurement sequence as follows: ● first day - fresh polish, ○ first day - baked specimens, ▲ second day - same bake, △ third day - same bake, ■ fourth day - fresh polish, □ eighth day - fresh polish.

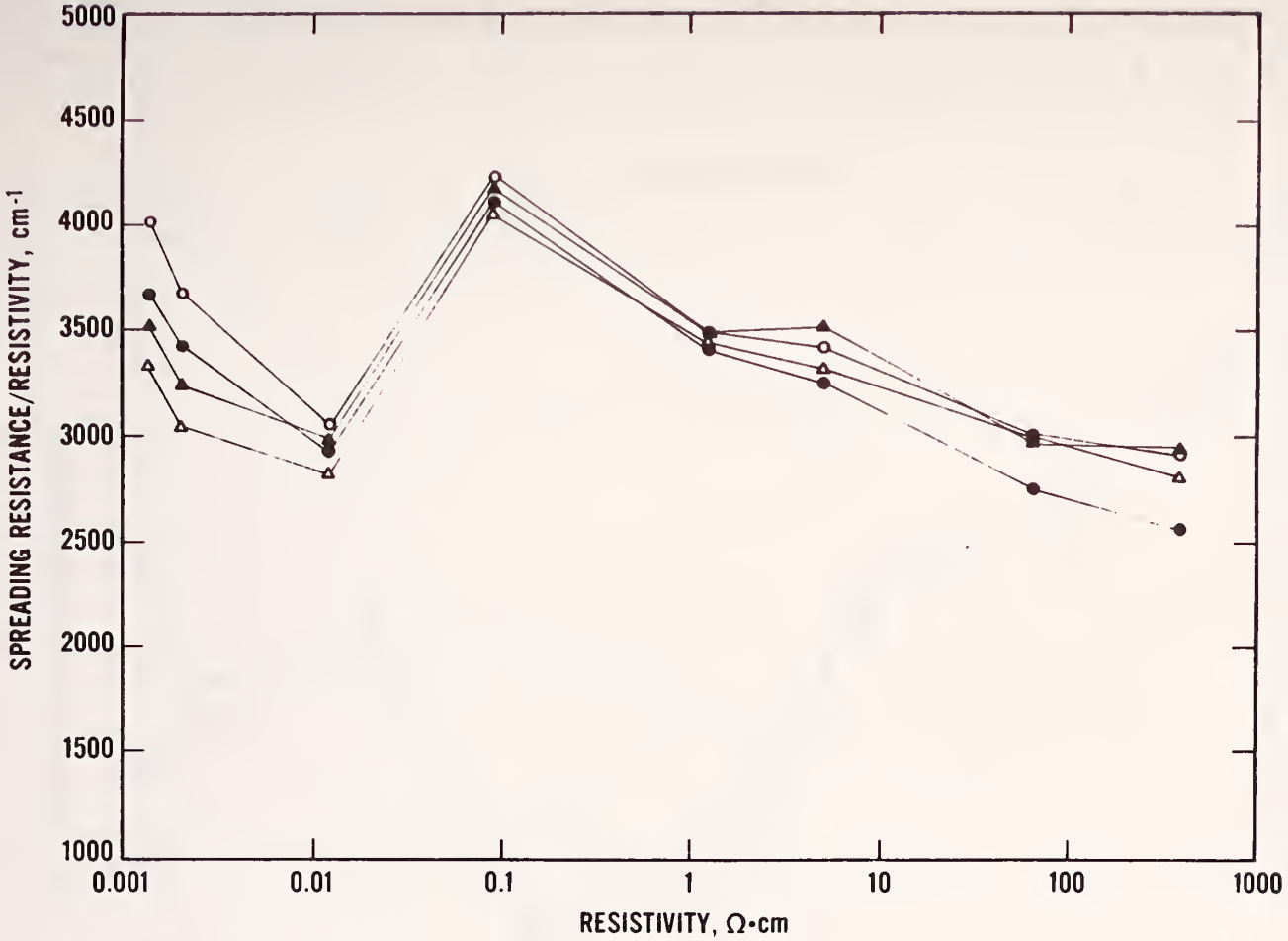

Figure D-3b. Calibration response for (111) n-type silicon polished with 0.5-μm diamond — probe set A (probe quality checked at three resistivity values). Measurement sequence as follows: ● first day - fresh polish, ○ second day - same polish, ▲ second day - fresh polish, △ third day - fresh polish.

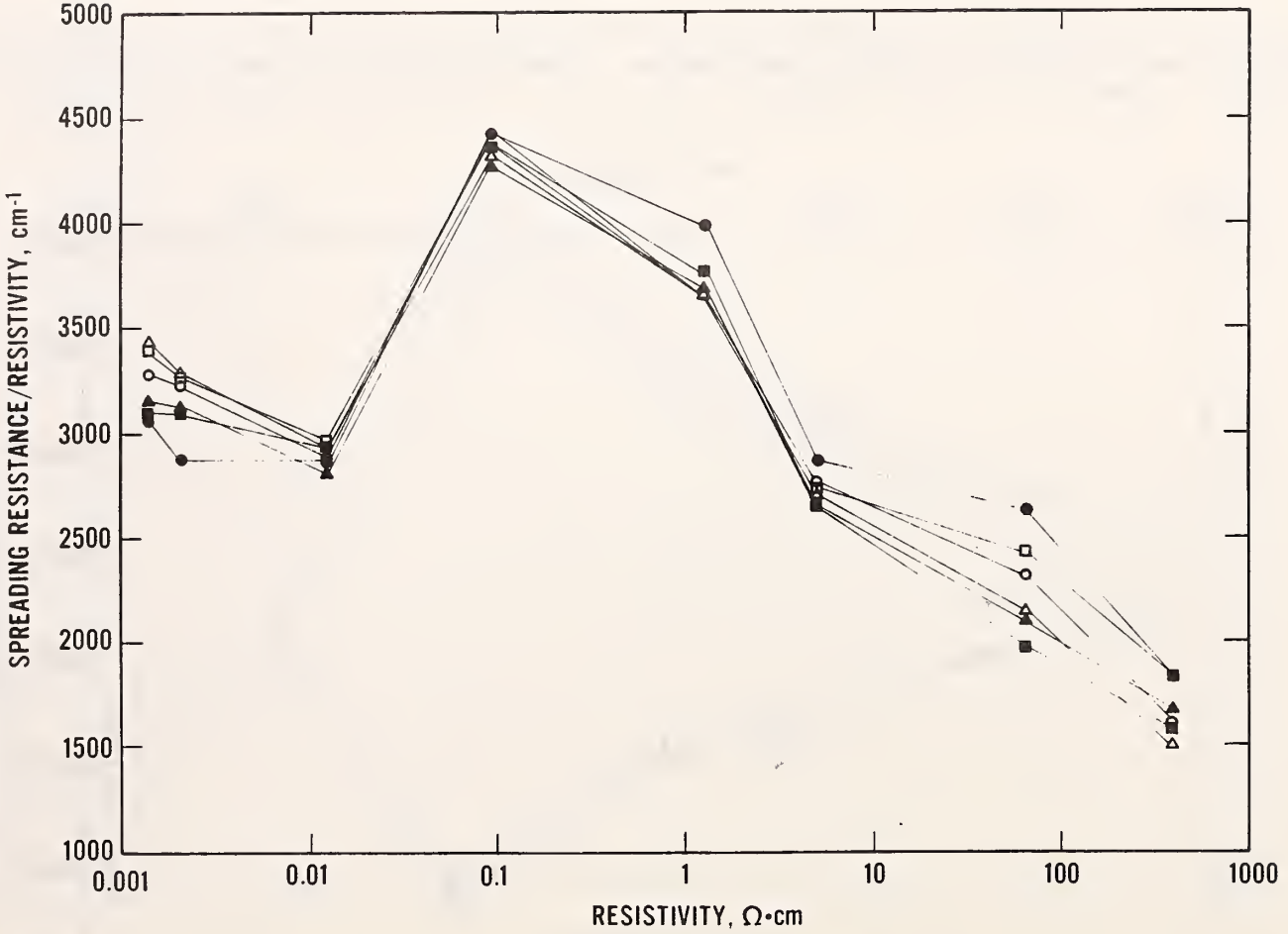

Figure D-3c. Calibration response for (111) *n*-type silicon polished with silica -- probe set A (probe quality checked at three resistivity values). Measurement sequence as follows: ● first day - fresh polish, ○ first day - baked specimens, ▲ first day - fresh polish, △ second day - baked specimens, ■ second day - fresh polish, □ second day - baked specimens.

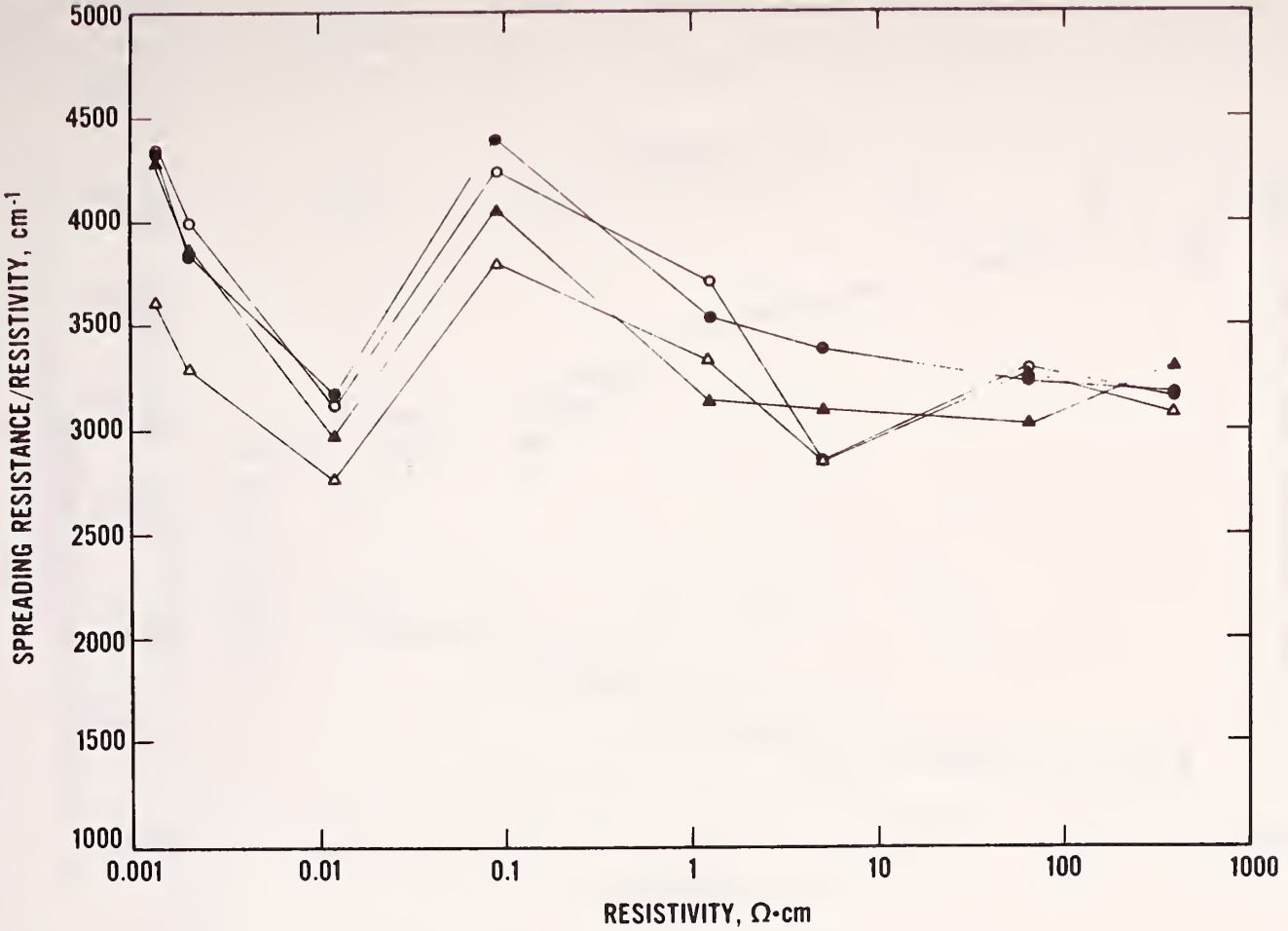

Figure D-3d. Calibration response for (111) *n*-type silicon — probe set B (probe quality checked at three resistivity values). Measurement sequence as follows: ● first day - 0.5-μm diamond polish, ○ first day - silica polish and baked, ▲ third day - 0.5-μm diamond polish, △ third day - silica polish.

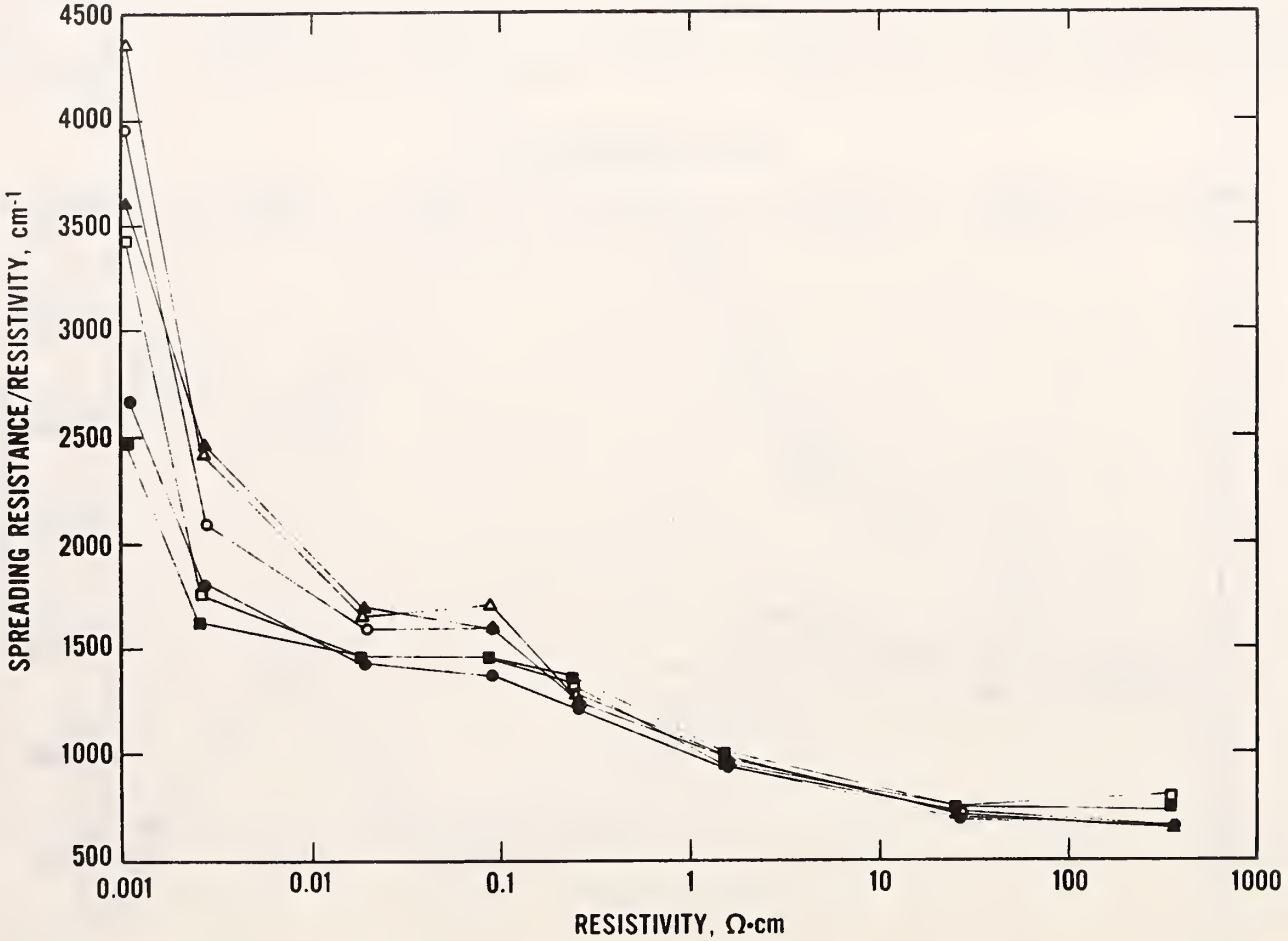

Figure D-4a. Calibration response for (111) p-type silicon polished with 0.5-μm diamond – probe set A (probe quality checked at mid-range resistivity only). Measurement sequence as follows: ● first day - fresh polish, ○ first day - baked specimen, ▲ second day - same baked surface, △ third day - same baked surface, ■ fourth day - fresh polish, □ seventh day - fresh polish.

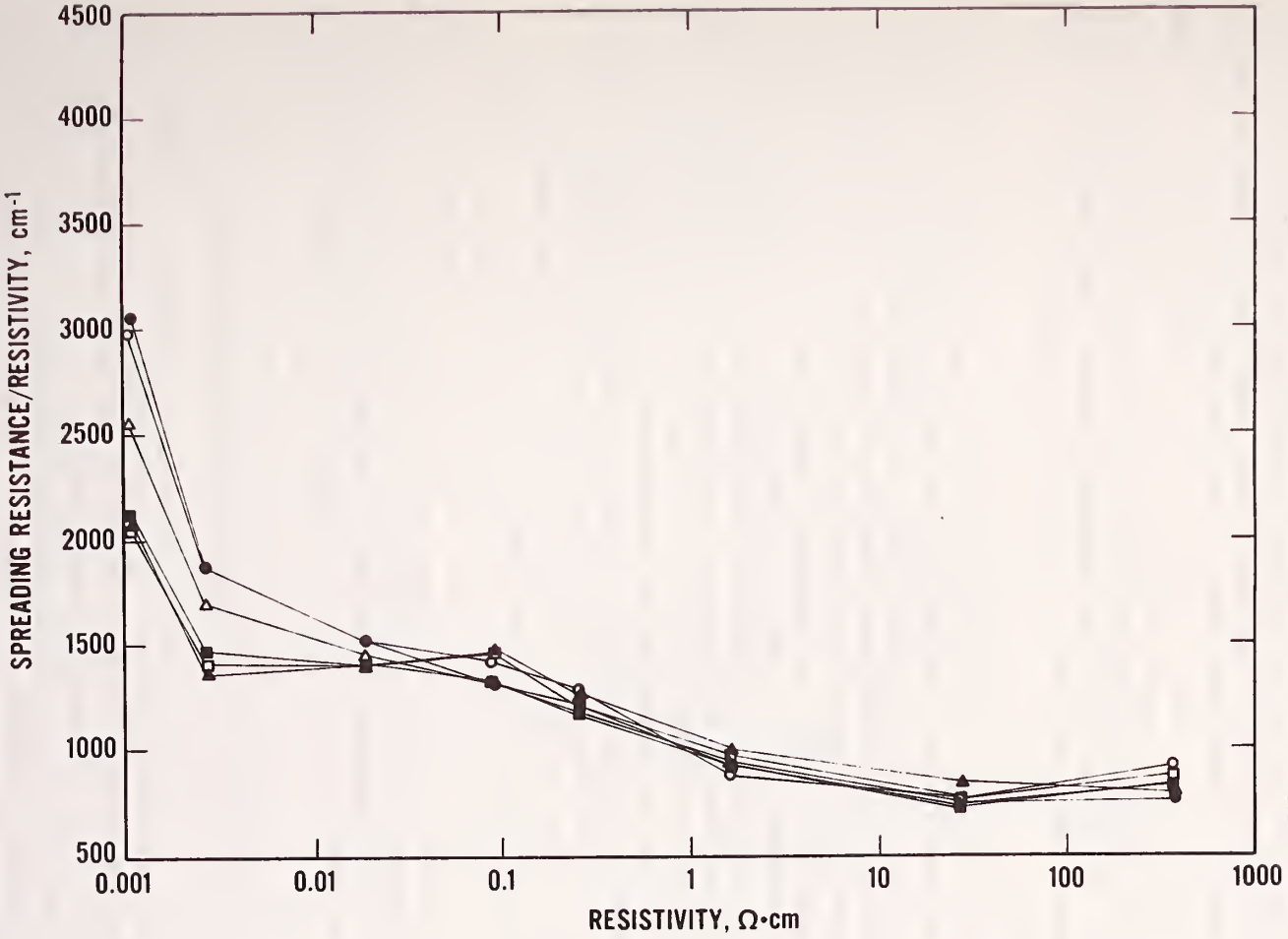

Figure D-4b. Calibration response for (111) p-type silicon (probe quality checked at three resistivity values). Measurement sequence as follows: Probe set A — ▲ first day - fresh silica polish and bake, △ first day - fresh 0.5-μm diamond polish, ■ third day - fresh diamond polish, □ third day - fresh silica polish and bake. Probe set B — ● first day - 0.5-μm diamond polish, ○ third day - fresh 0.5-μm diamond polish.

Differences found for (111) n-type calibration data as a function of specimen preparation can be broken into three parts as a function of specimen resistivity. For the lowest resistivity values (<0.01 Ω•cm), diamond-polished specimens yield higher (and less reproducible) spreading resistance values than do silica-polished specimens (with or without subsequent baking). In the mid-range of specimen resistivity (0.01 to 1 Ω•cm), the diamond-polished specimens show consistently lower spreading resistance values, again indicating a smaller effective barrier; the difference, however, is small. Above 1 Ω•cm, diamond-polished specimens have a noticeably more linear calibration than do silica-polished specimens. Further, it is seen by comparing figures D-3b and D-3c with figure D-3d that the nature of this relation appears less sensitive to the probes used when the specimens are diamond polished than when they are silica polished.

The increased spreading resistance values for low resistivity diamond-polished specimens is not, of itself, particularly significant. However, the degradation of reproducibility in calibration for low resistivity diamond-polished specimens, while not serious, should be noted. It may be related to residual scratch density on the silicon surface; the scratch density cannot be precisely controlled. It may also be due to increased sensitivity of such diamond-polished specimens to probe condition and cleanliness. Whatever the cause, it is perhaps advisable to use a low resistivity (111) n-type specimen to monitor probe condition as it relates to measurements on low resistivity n-type layers (thyristor cathode emitters, in the present case). Calibration data obtained on n-type specimens above 1 Ω•cm are somewhat surprising. Repeatability on diamond-polished specimens is not quite as good as expected based on the results in section C-4 and is not as sensitive to probe differences as was expected from previous work [D-1]. Further, repeatability on silica-polished specimens is not as bad as expected based on the results in section C-4. Nevertheless, repeatability of the calibration response for (111) n-type silicon above 1 Ω•cm is seen to be better for diamond-polished specimens than for silica-polished specimens. Calibration response on all other diamond-polished specimens is seen to be acceptably repeatable for application of diamond beveling to depth profiling.

D-3 Special Modification for Large Angle Beveling of Thyristors

Depth profiling of actual thyristor structures was found to require an additional process modification. Typical thyristor structures require sectioning to a depth from about 100 to 150 μm to gain the information needed. This generally requires a beveling angle of 3 to 10 deg. Regardless of beveling angle used (5 deg was the nominal angle for measurements of actual thyristor profiles), a considerable volume of silicon must be removed. Both 0.5- and 0.1-μm diamond are too fine to remove the required amount of material in a reasonable time, so a multistage process was used. In the first stage, the specimen was rough beveled with 5-μm aluminum oxide against a glass plate, a process which took about two minutes per specimen. The specimen and bevel block were

thoroughly cleaned and transferred to a separate piston and collar (see fig. 3-1a) to minimize contamination of the subsequent diamond polishing with coarser aluminum oxide. Diamond polishing followed in two stages, first using 0.5-μm diamond to rapidly remove the damage caused by aluminum oxide and then using 0.1-μm diamond for the desired surface finish. The specimen and bevel block were dismounted from piston and collar and all parts thoroughly cleaned between the two stages of diamond polishing.

This diamond-beveling process has two potential difficulties. First, dismounting and remounting of specimen and beveling block from piston and collar for purposes of cleaning can result in small changes of working angle unless all components have perfect alignment. These changes in working angle result in slight changes in, or faceting of, the beveled surface which slows the beveling process. Second, excessive scratching was often noted during the final 0.1-μm polishing. While this was at first believed due to incomplete removal of previous coarser grit compound, it was also noted that the open end of the beveled surface had a strong tendency to chip, perhaps due to damage during the original coarse beveling with aluminum oxide. The problem was reduced, but not eliminated, by very careful cleaning of the frosted glass plate and replenishment of the diamond slurry for each specimen and sometimes during the course of finishing any one specimen. The result is that the final surface finish of the specimen was generally not as good as was obtained when beveling at shallower angles where 0.1-μm diamond alone be used. Somewhat excessive scatter in the spreading resistance data of the thyristors may be due to the surface quality.*

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*Subsequent to the acquisition of thyristor profile data discussed in section D-4, additional tests of the beveling process were conducted. In these tests it was found possible to go directly from the initial beveling with 5-μm alumina to final finishing with 0.1-μm diamond, thus eliminating the intermediate 0.5-μm diamond step previously required. The quality of the specimen surfaces obtained with the two-step process was, in general, superior to that obtained previously with the three-step beveling process.

To accomplish this process change, it was necessary to remachine the reference surfaces of the polishing collars used during beveling so that this surface was perpendicular to the bore of each collar (separate collars and pistons are used for each beveling abrasive to minimize cross-contamination). In addition, viscous optical grease was applied to the bore of the collars to maintain the pistons in tight alignment during beveling. These changes to the beveling apparati reduce or eliminate the small changes in beveling angle, previously experienced as faceting, when the beveling block and specimen are transferred from one piston-collar set to another.

D-4 Thyristor Depth Profiling by Spreading Resistance Measurement

Spreading resistance depth profiles were taken on chips cut from three different thyristors. Thyristor I was laboratory fabricated, and thyristors II and III were taken from production runs. Two chips were cut from each thyristor. One chip was rough beveled with aluminum oxide, bevel polished with 0.5-μm diamond, and then repolished with 0.1-μm diamond, with spreading resistance profiles being taken after both the 0.5- and 0.1-μm diamond steps. The other chip was also rough beveled with aluminum oxide, finished with colloidal silica, and then baked for 15 min at 150°C; spreading resistance profiles were taken both before and after baking.

In this manner, it is possible to test the relative response of the 0.1-μm diamond-finished surfaces against the responses resulting from the other surface preparations. Note that, from the preliminary tests discussed in section D-2, 0.1-μm diamond bevel-polishing against glass was found to result in data equivalent to those from 0.5-μm diamond top surface polishing against a compliant polishing pad. This latter process, in turn, was demonstrated to give repeatability for high resistivity n-type silicon. Note also, with respect to silica polishing, that the subsequent thermal treatment of specimens has been found to be necessary for proper repeatable interpretation of p-type layers [D-1,D-2] but that there is no clear advantage of such thermal treatment for interpretation of n-type layers.

Data for all depth profiles were analyzed using the "local slope" algorithm of Dickey [D-5] to account for the effect on the data of layer gradation and underlying junctions. Spreading resistance calibration was applied by using the simple log-log relation for empirical calibration data:

$$\log R_{SP} = b + m \log \rho \ , \qquad \text{(D-1)}$$

where R_{SP} is the spreading resistance, ρ is the resistivity of a calibration specimen, and b and m are the intercept and slope, respectively, of a straight line fit of the empirical calibration. This relation is applied to depth profile data using the form:

$$\rho = (R_C \times 10^{-b})^{1/m} \ , \qquad \text{(D-2)}$$

where the values, R_C, of spreading resistance used in the equation are those obtained from application of the sampling volume correction to the as-measured spreading resistance to account for the effect of layer structures [D-5]. Since the particular structures of two of the thyristors used (designated thyristor II and thyristor III) are considered proprietary by their suppliers, measurements on them will be given only in normalized tabular form. The only graphical data presented for a full profile are those for thyristor I and are found in figures D-5 to D-8. Part (a) of each figure shows an overview of the structure taken at probe step increments of 25 μm. Part (b) of the figures give better

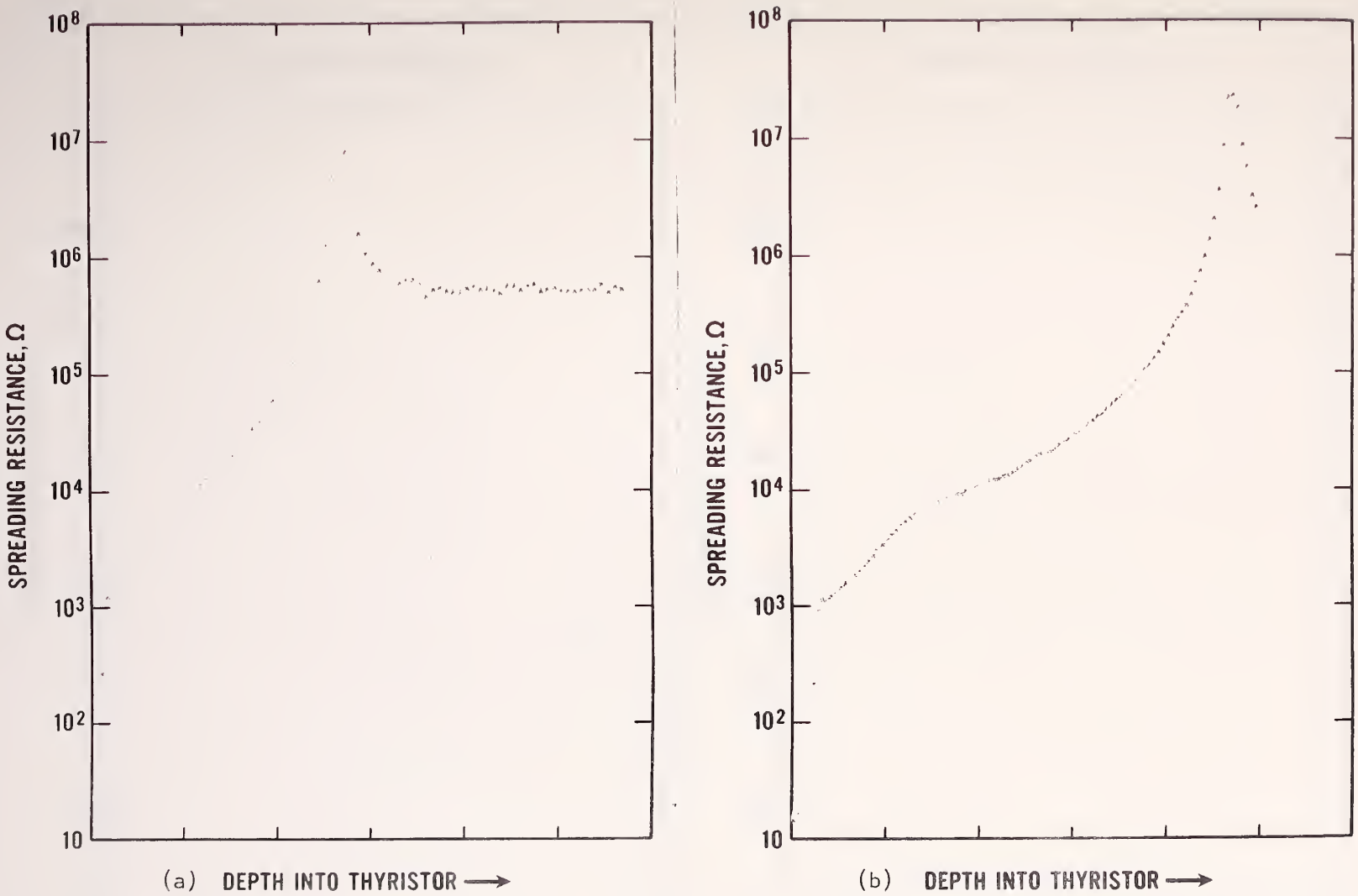

Figure D-5. Raw data for cathode emitter, *p*-base and part of *n*-base: thyristor I, 0.5-μm diamond-beveled specimen. (a) 25-μm step size, (b) 10-μm step size.

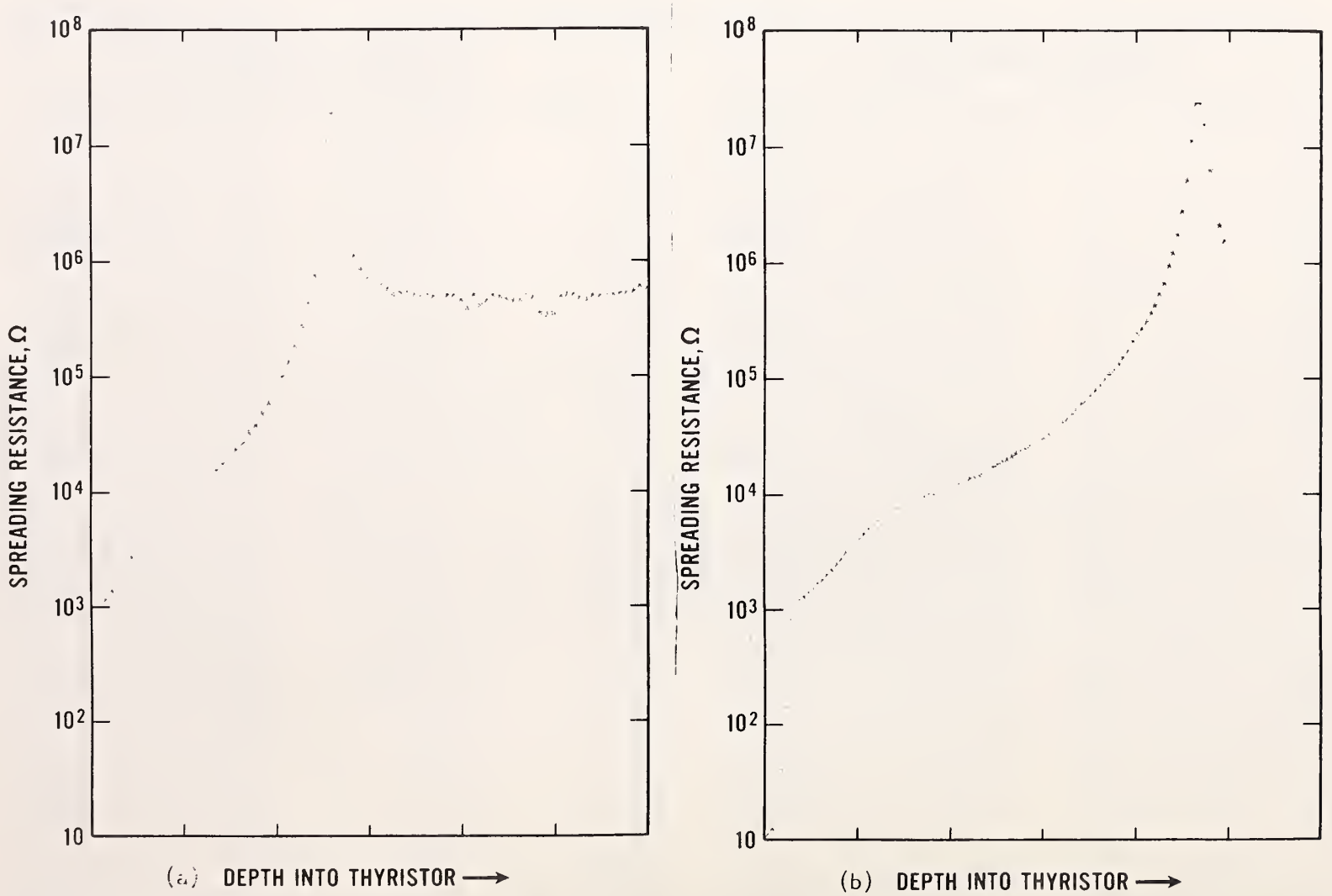

Figure D-6. Raw data for cathode emitter, *p*-base and part of *n*-base thyristor I, 0.1-μm diamond-beveled specimen. (a) 25-μm step size, (b) 10-μm step size.

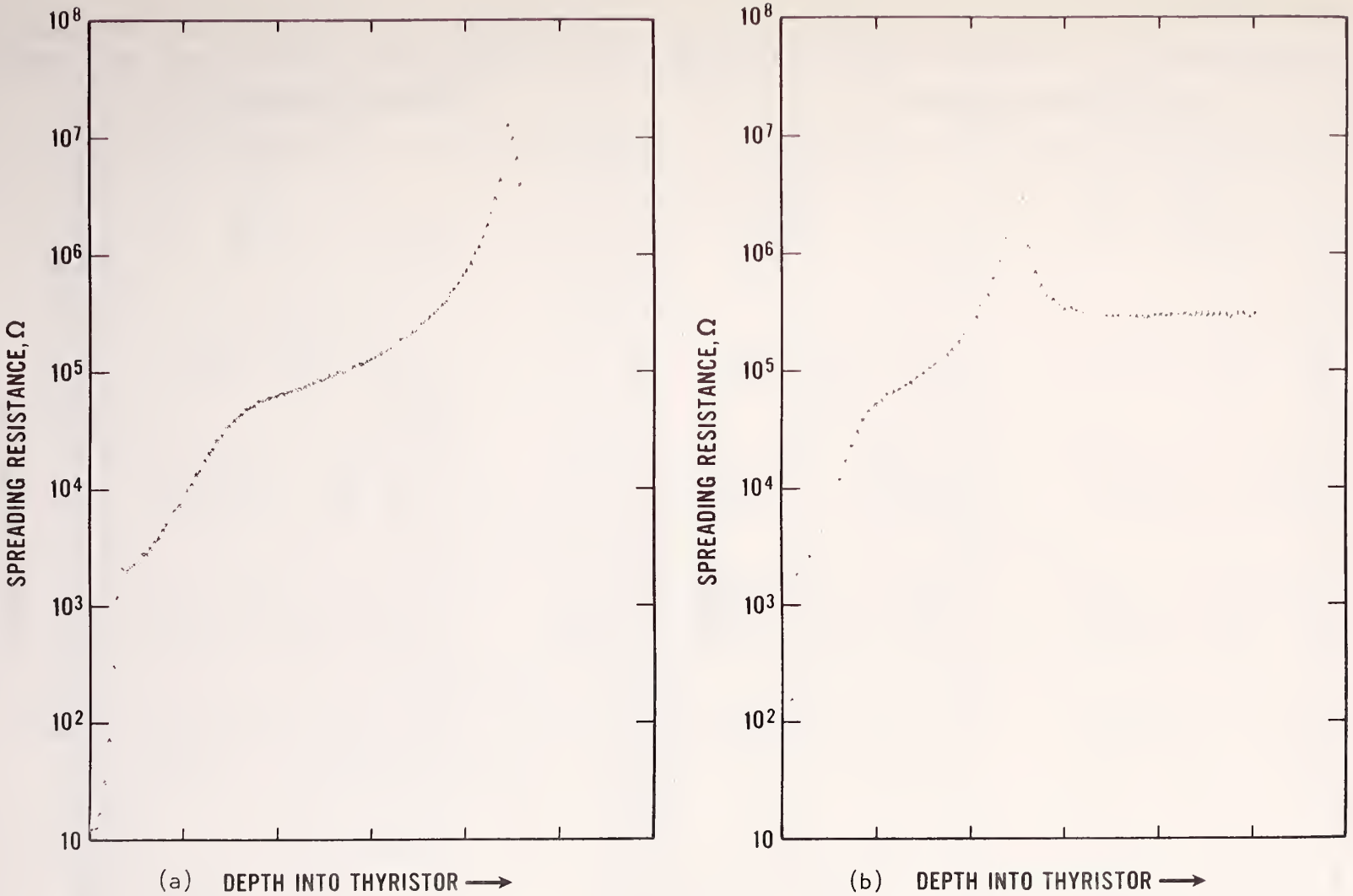

Figure D-7. Raw data for cathode emitter, p-base and part of n-base thyristor I, colloidal silica-beveled specimen. (a) 25-μm step size, (b) 10-μm step size.

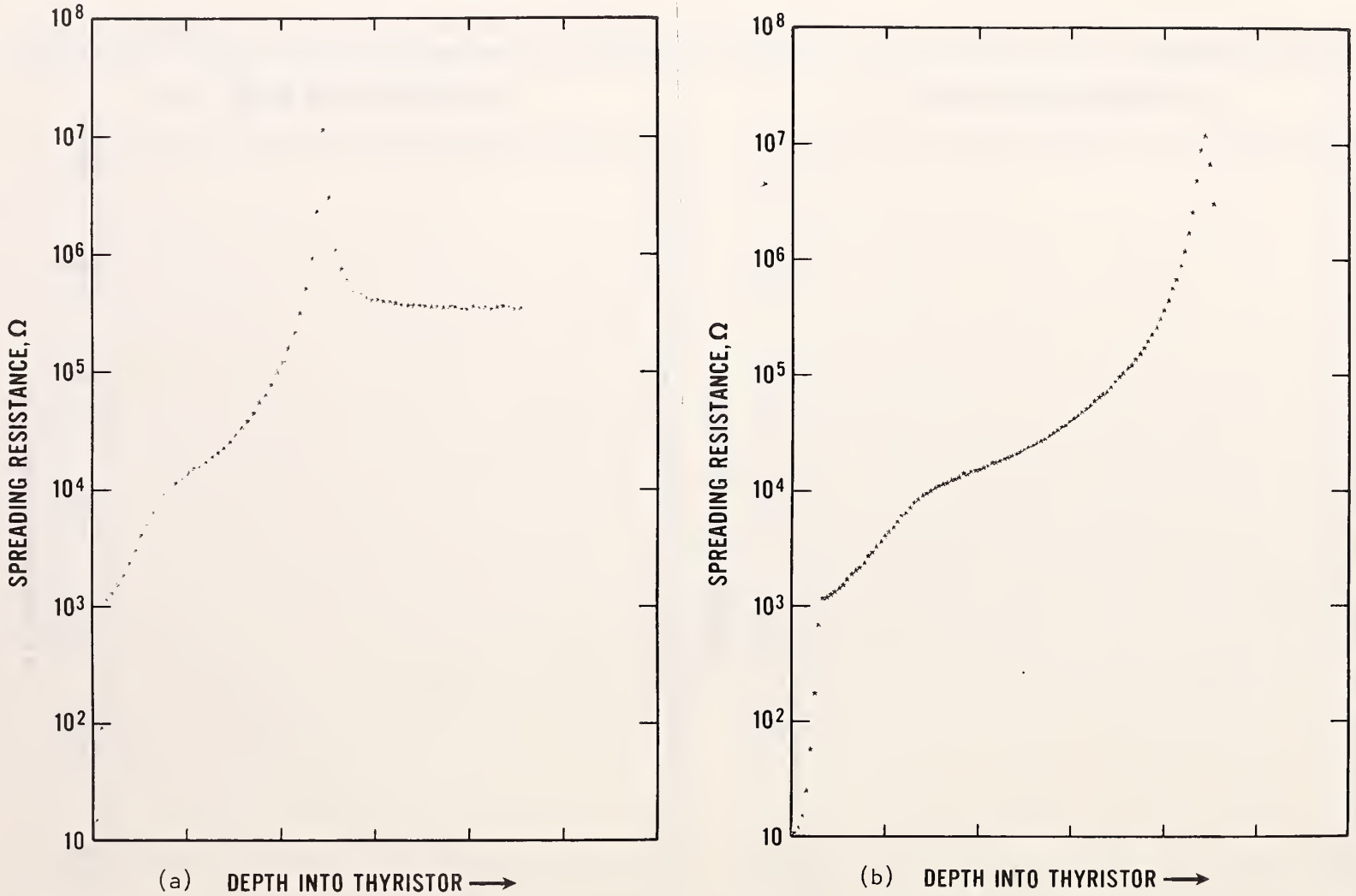

Figure D-8. Raw data for cathode emitter, p-base and part of n-base thyristor I, colloidal silica-beveled and baked specimen. (a) 25-μm step size, (b) 10-μm step size.

Table D-2. Ratios of Thyristor Parameters Obtained with Various Surface Preparations to the Values Obtained with 0.1-μm Diamond-Polished Surfaces — Thyristor I.

	N_{max}	Rs(N)	P_{max}	Rs(P)	ρ_{subst}
0.1-μm diamond	1	1	1	1	1
0.5-μm diamond	0.75	1.52	1.06	0.94	1.08
Silica	1.0	1.29	0.61	2.01	0.6
Silica + bake	1.0	0.94	1.06	1.04	0.73

Table D-3. Ratios of Thyristor Parameters Obtained with Various Surface Preparations to the Values Obtained with 0.1-μm Diamond-Polished Surfaces — Thyristor II.

	N_{max}	Rs(N)	P_{max}	Rs(P)	ρ_{subst} *
0.1-μm diamond	1	1	1	1	1
0.5-μm diamond	0.89	1.02	1.11	1.00	1.25
Silica	0.91	1.06	0.61	1.70	0.95
Silica + bake	0.79	1.08	1.00	0.95	0.75

* The values obtained for *n*-base resistivity on the diamond-beveled specimens were within 10 percent of the manufacturer's process value on the two specimens for which it was known.

Table D-4. Ratios of Thyristor Parameters Obtained with Various Surface Preparations to the Values Obtained with 0.1-μm Diamond-Polished Surfaces — Thyristor III.

	N_{max}	Rs(N)	P_{max}	Rs(P)	ρ_{subst} *
0.1-μm diamond	1	1	1	1	1
0.5-μm diamond	0.9	0.93	0.93	0.96	1
Silica	0.85	0.94	0.49	2.31	0.90
Silica + bake	0.75	1.04	0.93	1.14	0.70

* The values obtained for *n*-base resistivity on the diamond-beveled specimens were within 10 percent of the manufacturer's process value on the two specimens for which it was known.

definition to the cathode emitter and was obtained with 10-μm probe steps. A summary of the normalized data for the three thyristors is given in tables D-2 to D-4. In the tables, the maximum carrier concentration and sheet resistance are given for the cathode emitter, the maximum carrier concentration and sheet resistance are given for the p-base, and the average resistivity is given for the n-base. Carrier concentrations for the n-type layer and for the p-type layer are derived from the resistivity profiles using the relations of Caughey and Thomas [D-6] and of Wagner [D-7], respectively. The values of each of these parameters, as obtained from the 0.1-μm diamond-polished specimens, are assigned the value unity. Values of the parameters obtained with the other specimen preparations are expressed as a ratio (to unity).

For each of the specimen surfaces tested, the general quality of the data shown in figures D-5 through D-8 for thyristor I is very similar to that obtained for the same type surface on the other two thyristors. Qualitatively, it can be seen from figures D-5 through D-8 for thyristor I that all four surface preparations yield data with low scatter for the cathode emitter and the p-base layers. Data from the diamond-polished specimens for the n-base show slightly more scatter than those from the silica-polished specimens. This scatter, related to excess scratching sometimes encountered in diamond beveling, is not serious, and its existence is more than compensated by improved accuracy of the average n-base resistivity obtained on diamond-beveled specimens. The general shape for the cathode emitter is seen to be the same for all four specimens from thyristor I. For the p-base layer, good agreement on shape is found for all preparations but the simple silica polish. Such a difference is expected for nonbaked silica-polished p-type layers based on previous results [D-1,D-2]. (Apparent differences in depth of the p-base are due to differences in bevel angle among the several specimens.) The average n-base (substrate) resistivity has a consistent value for the two diamond-polished specimens, but this value differs with values found from each of the silica-polished specimens. This finding regarding consistency of interpretation of high resistivity n-layers is in agreement with the results in section C-4.

D-5 Summary of Depth Profiling

The purpose of these tests was to investigate the extension of diamond polishing to depth profiling of thyristor devices. Such extension, if successful, should be evidenced by superior interpretation of average n-base resistivity compared to the value obtained from silica-beveled (or silica-beveled and baked) specimens. Since previous work [D-2] indicates that silica (or other aqueous) polishes should be followed by baking for proper interpretation of p-type (p-base) layers, results from the silica-beveled and baked specimens will be used for comparison to judge the success of diamond beveling on p-type layers. Lastly, since no clear evidence for the need of baking has yet been developed for proper interpretation of highly doped n-type layers (cathode emitter), results from both baked and unbaked specimens were used for comparison

to test the quality of results of diamond beveling on highly doped n-type layers.

Practical considerations make it desirable to use just a single surface preparation which is satisfactory for both p- and n-type layers. The best such process for overall comparison with diamond beveling is silica beveling followed by baking because of the known advantages for interpretation of p-type layers. Data from silica-beveled but unbaked specimens should also be in reasonable agreement for the cathode emitter but noticeably in error for the p-base. Data from the 0.5-μm diamond-beveled specimens may be in good agreement with those from 0.1-μm diamond-beveled specimens for all layers. However, if discrepancies are found, they are expected to be due to the tests discussed in section D-2 regarding the applicability of calibration to specimens which have been beveled with 0.5-μm diamond. This point will be discussed further below.

The principal question that may be raised regarding interpretation of the diamond-polished specimen profiles reported in the preceding section is that of the appropriateness of the calibration procedure used for the diamond-beveled specimen. The composite resitivity calibration block was polished with 0.5-μm diamond against the nonwoven polishing cloth described in section C-1. Spreading resistance measurements taken on the top surface of the specimen chips in this block and a knowledge of the chip resistivities constituted the calibration data used for interpretations of profiles from specimens beveled with 0.1-μm diamond against frosted glass. Because spreading resistance measurements are known to depend on specimen preparations, conventional good practice requires that calibration specimens be prepared in exactly the same manner as the test specimen to be evaluated. This suggests that, if the test specimen is to be beveled at a certain angle, all calibration specimens be beveled at the same angle; it also suggests that the final beveled surface area be the same on test and calibration specimens so that possible differences due to pressure during polishing are eliminated. However, carried to a literal extreme, such calibration practice becomes untenable since brand new calibration specimens would be required regularly to meet changing requirements on bevel angle, surface area prepared, etc. More realistically, compromise calibration procedures are necessary and are commonly used. To utilize any such compromise procedure and maintain an acceptable level of measurement uncertainty, it is necessary to validate the procedure chosen. In the present case, such a validating test was reported in section D-2. The results of the test showed that both p- and n-type (111) silicon specimens over nearly 6 decades of resistivity had the same spreading resistance response (within 5 percent) for measurements on surfaces beveled with 0.1-μm diamond against frosted glass and for measurements on surfaces polished with 0.5-μm diamond against a nonwoven cloth polishing pad. This is taken as a functional verification of the use of calibration data obtained on specimens polished with 0.5-μm diamond and a soft cloth for interpreting data on specimens beveled with 0.1-μm diamond on frosted glass. An alternate procedure for preparing calibration specimens would, of course,

be to polish them directly with 0.1-μm diamond against frosted glass. This might be difficult for large area calibration specimens if they were not sufficiently flat; in this case, they could be beveled at a shallow angle with 0.1-μm diamond against frosted glass, in the manner of a specimen to be depth profiled. Either of these alternate procedures for preparing calibration specimens should assure formal, as well as functional, equivalence with specimens to be depth profiled. Because of the construction chosen for the composite calibration block, neither of the alternate procedures could be applied in the present case.

The data depicted in tables D-2 to D-4 for the cathode emitter show that 0.1-μm diamond polishing compares acceptably well with silica polishing followed by baking, when the limitations imposed by the number of data points obtainable for this layer are taken into consideration. Somewhat better agreement between the results from 0.1-μm diamond and those from silica only is also noted. The tables also show a good agreement between the baked silica-polished and 0.1-μm diamond-polished specimens regarding p-base parameters.

It is concluded, therefore, that there is a definite advantage to be gained from using nonaqueous 0.1-μm diamond polishing for beveling of thyristor structures. Note that the generally favorable measurements of all layers on the 0.5-μm diamond-polished specimens may be fortuitous because of the possible inapplicability of the calibration obtained on surfaces polished with 0.5-μm diamond against a soft pad to specimens beveled with 0.5-μm diamond against frosted glass. Note also that the measurement quality obtained on thyristors beveled with 0.1-μm diamond should also be obtained on other device structures beveled in the same manner. Since shallow angles (1 deg or less) can be beveled in a single step with 0.1-μm diamond, the problem of controlling surface quality, noted in section D-3 for multiple step beveling, should be eliminated. Moreover, for the case of relatively shallow structures, such as those found in integrated circuits, the additional benefit of very sharp bevel intersection with the top surface is obtained from diamond beveling.

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NBS-114A (REV. 9-78)

U.S. DEPT. OF COMM. BIBLIOGRAPHIC DATA SHEET	1. PUBLICATION OR REPORT NO. NBSIR 79-1756	2. Gov't Accession No.

4. TITLE AND SUBTITLE

Measurement Techniques for High Power Semiconductor Materials and Devices:

Annual Report, October 1, 1977 to September 30, 1978

5. Publication Date

June 1979

7. AUTHOR(S)

Frank F. Oettinger, Editor

8. Performing Organ. Report No.

9. PERFORMING ORGANIZATION NAME AND ADDRESS

NATIONAL BUREAU OF STANDARDS
DEPARTMENT OF COMMERCE
WASHINGTON, DC 20234

11. Contract/Grant No.

Task Order A021-EES;
NBS/DOE EA-77-A-01-6010

12. SPONSORING ORGANIZATION NAME AND COMPLETE ADDRESS *(Street, City, State, ZIP)*

Department of Energy
Division of Electric Energy Systems
Washington, DC 20545

13. Type of Report & Period Covered

October 1, 1977 to
September 30, 1978

15. SUPPLEMENTARY NOTES

Results of related studies funded by the Defense Advanced Research Projects Agency through Order No. 2397 and by the NBS are also reported herein for completeness.

☐ Document describes a computer program; SF-185, FIPS Software Summary, is attached.

16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

This annual report describes NBS activities directed toward the development of measurement methods for semiconductor materials and devices which will lead to more effective use of high power semiconductor devices in applications for energy generation, transmission, conversion, and conservation. It responds to national needs arising from rapidly increasing demands for electricity and the present crisis in meeting long-term energy demands. Emphasis is on the development of measurement methods for thyristors and rectifier diodes.

The major tasks under this project are (1) to evaluate the use of thermally stimulated current and capacitance measurements and other deep level measurement techniques as a means for characterizing lifetime controlling or leakage source defects in power grade silicon material and devices, and (2) to develop procedures to enable spreading resistance measurements of thyristor starting material and layer profiles to be made on a reliable basis.

17. KEY WORDS *(six to twelve entries; alphebetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

D-c transmission; deep level measurements; energy conservation; measurement methods; power-device grade silicon; resistivity variations; silicon; spreading resistance measurements; thermally stimulated measurements; thyristor materials measurements; thyristor measurements.

18. AVAILABILITY

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[X] Order From National Technical Information Service (NTIS), Springfield, VA, 22161

19. SECURITY CLASS (THIS REPORT)	21. NO. OF PRINTED PAGES
UNCLASSIFIED	146
20. SECURITY CLASS (THIS PAGE)	**22. Price**
UNCLASSIFIED	$7.25

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